CBTech(1595) Investor Conference 2025/12/19

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Disclaimer

This presentation, which included statements regarding its results of operations, financial conditions, and business prospects, are only based on the Company' s estimates and expectations and are for reference only. Any business outlook or forward-looking statement hereof is subject to change after this date. Except as required by law, we undertake no obligation to update any forward-looking statement, whether as a result of new information, future events, or otherwise.

Outline

- Introduction to the Company and its Existing Products
- Overview and Business Model of TGV Glass Substrate Market
- CBTech
  1. TGV Glass Substrate Metallization Manufacturing Line
  2. Photomask AOI
- Subsidiary- BHT
  1. Semi Equipment PEALD/PEALE
  2. Front, Back-End IC Test & Packaging
- Q & A

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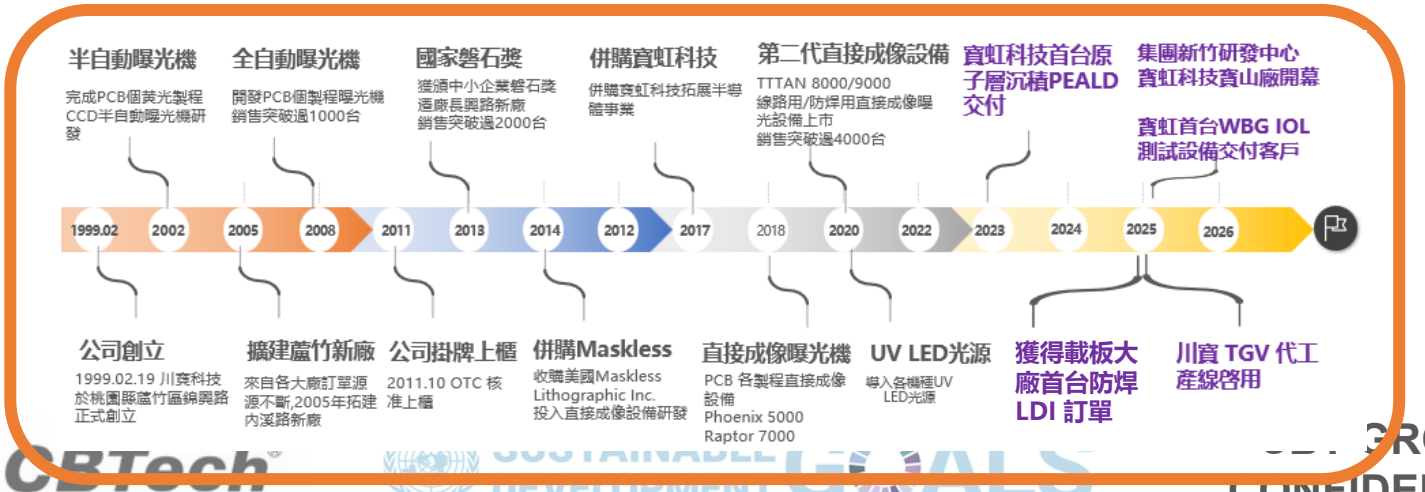
Introduction

Established: February 1999
Paid-in Capital: NT$541,995,000
Industry Position: A leading manufacturer of exposure equipment for the PCB and optoelectronics industries in Taiwan.
Main Products: Rotary exposure machines, direct-image exposure machines without photomasks, AOI and AVI automatic visual inspection systems.
Performance: Customers include Zhen Ding, HannStar, Tripod, Kingboard Chemical Group, KCE, Chicony Technology, APEX, Shenghong, etc., with a cumulative global equipment sales of over 5,000 units.

Stock Code: 1595
Awards and Honors:
2012 National Rock Award
Ranked 34th in the 2019 Top 5000 Large Enterprises Ranking - Specialized Manufacturing Machinery Industry
Passed the A+ Enterprise Innovation R&D Refinement Program “Next-Generation Circuit Board Prototype Rapid Manufacturing and Equipment Integration Development Program”



Existing Products

- LDI For PCB & Substrate
- Lead Frame & Substrate AVI
- Refurbished Semi Equipment & Spare Parts
- Fab Automation Tool.

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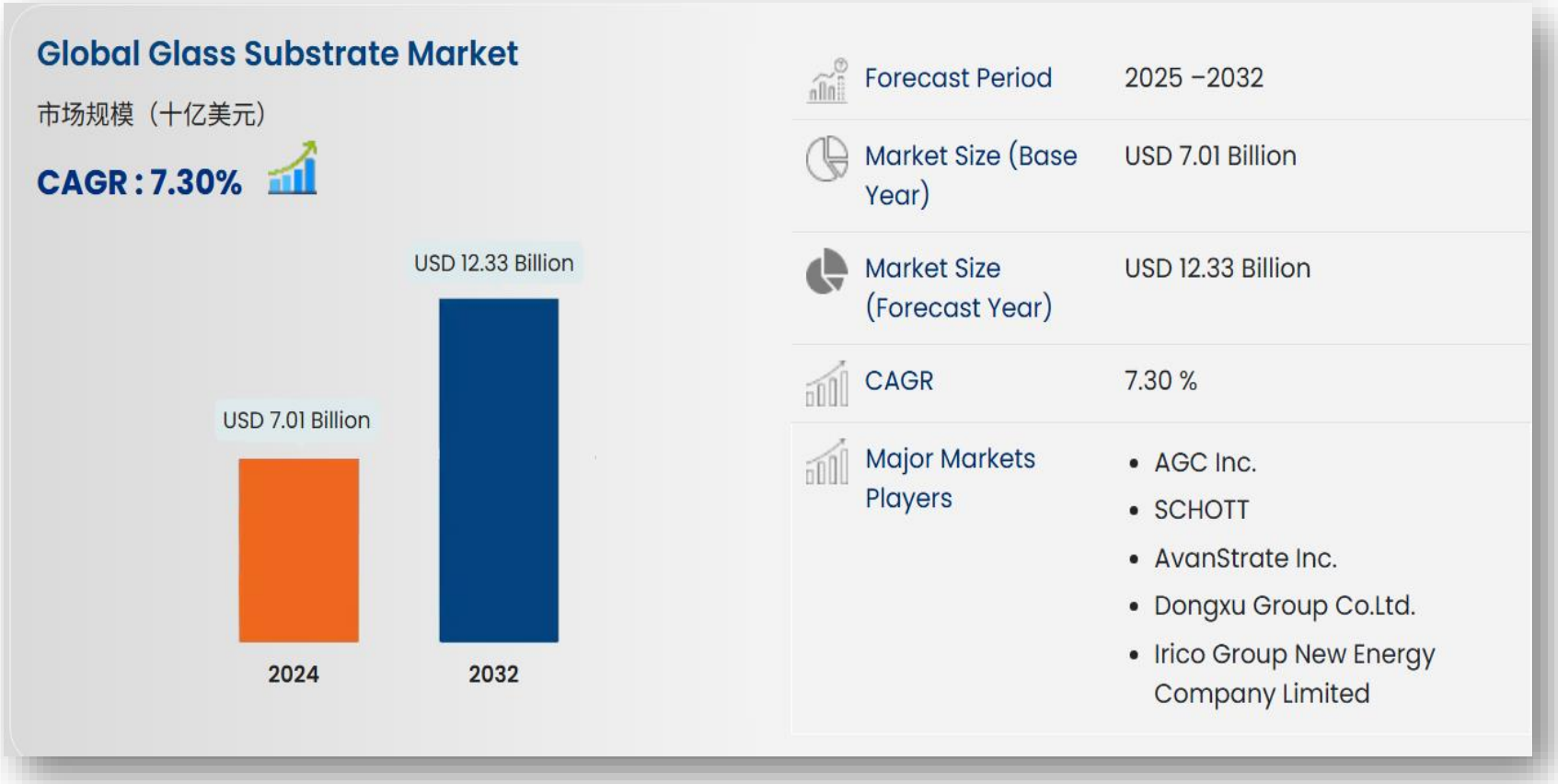
Market Trends and Size

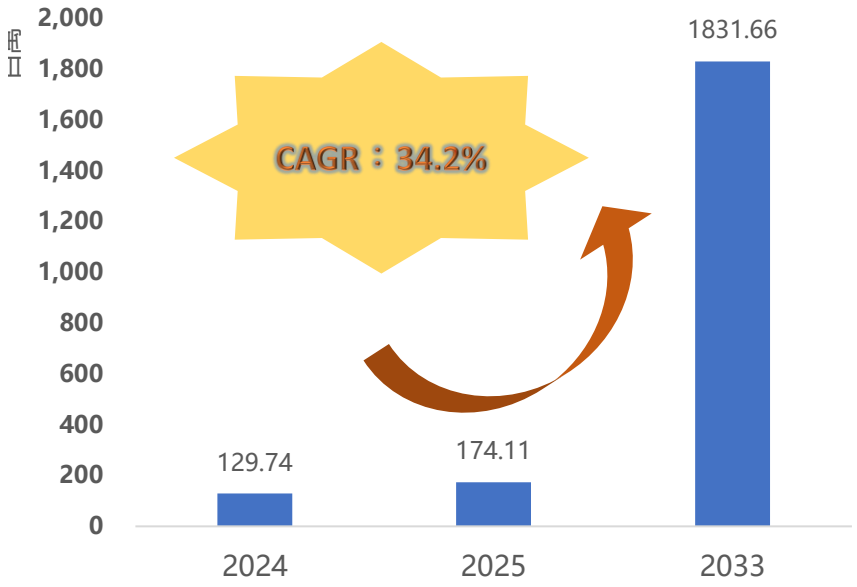
Market Trends and Size



- **Various research institutions indicate that the glass substrate market is worth billions to tens of billions of US dollars annually.**

The TGV glass substrate market is projected to reach $175 millions US dollars by 2025.

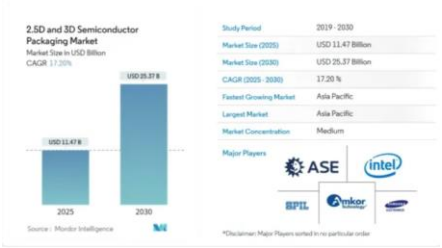
- The global market value of TGV glass substrates was US$130 millions in 2024, and is projected to reach US$175 millions by 2025, expanding to US$1.8 billions by 2033. The compound annual growth rate (CAGR) from 2025 to 2033 is 34.2%.



Industry Scale Growth Trend

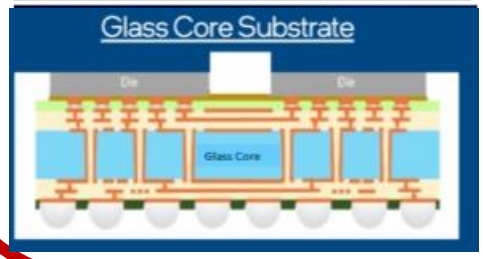
The global TGV/TSV 2.5D/3D packaging market is growing at a CAGR of 17.2%

Driven by the miniaturization of electronic devices and the demands of 5G and AI for high-speed and efficient computing, high bandwidth, low latency, and low power consumption, the global 2.5D/3D packaging market (including TGV/TSV packaging technologies) is predicted to grow at a very high rate, reaching $25.37 billion by 2030 with a CAGR of 17.2%, after reaching $11.47 billion in 2024. The proportion of TGV replacing TSV depends mainly on the adoption progress of major chip design companies (such as NVIDIA and AMD), with a penetration rate estimated to reach 20% between 2028 and 2030, a CAGR of over 20%



Glass Core Substrate With a 24.7% CAGR

The global TGV technology market is projected to grow from $63 million in 2024 to $238.4 million in 2030, representing a CAGR of 24.7% during the forecast period. Major global TGV technology vendors include Corning, LPKF, Samtec, Kiso Micro Co., Ltd., and Tecnisco. The top five vendors globally hold over 70% market share. The Asia-Pacific region is the largest market, with a share exceeding 15%, followed by Europe and North America.

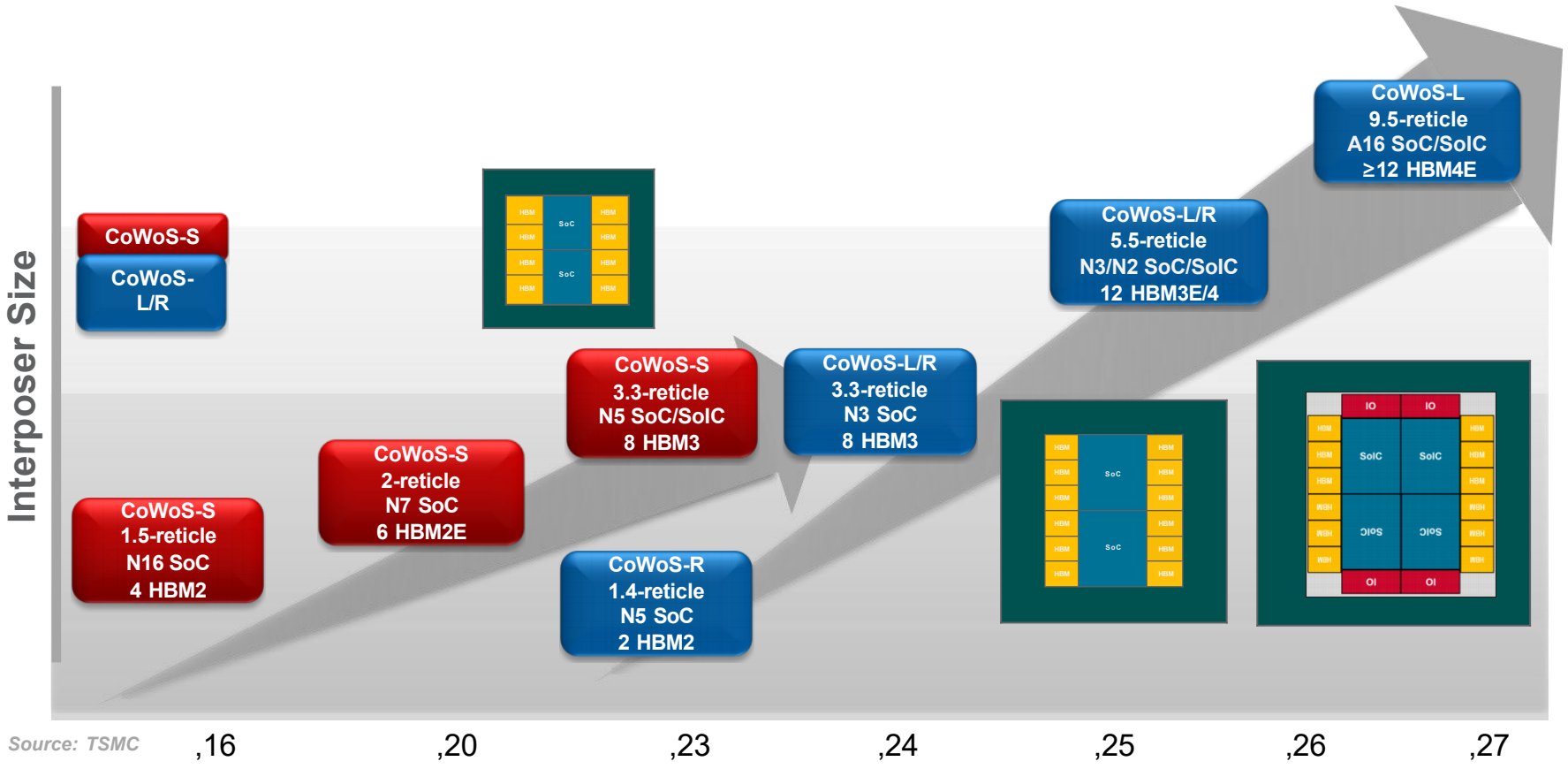


Mini LED backlight modules With a 13.5% CAGR

The Mini LED backlight product market is projected to grow from $720 million in 2024 to $2.1 billion in 2032. The CAGR for the Mini LED backlight product market is estimated at approximately 13.5% during the forecast period (2025-2032).

The red section are the main target products of the CBTech TGV OEM line.

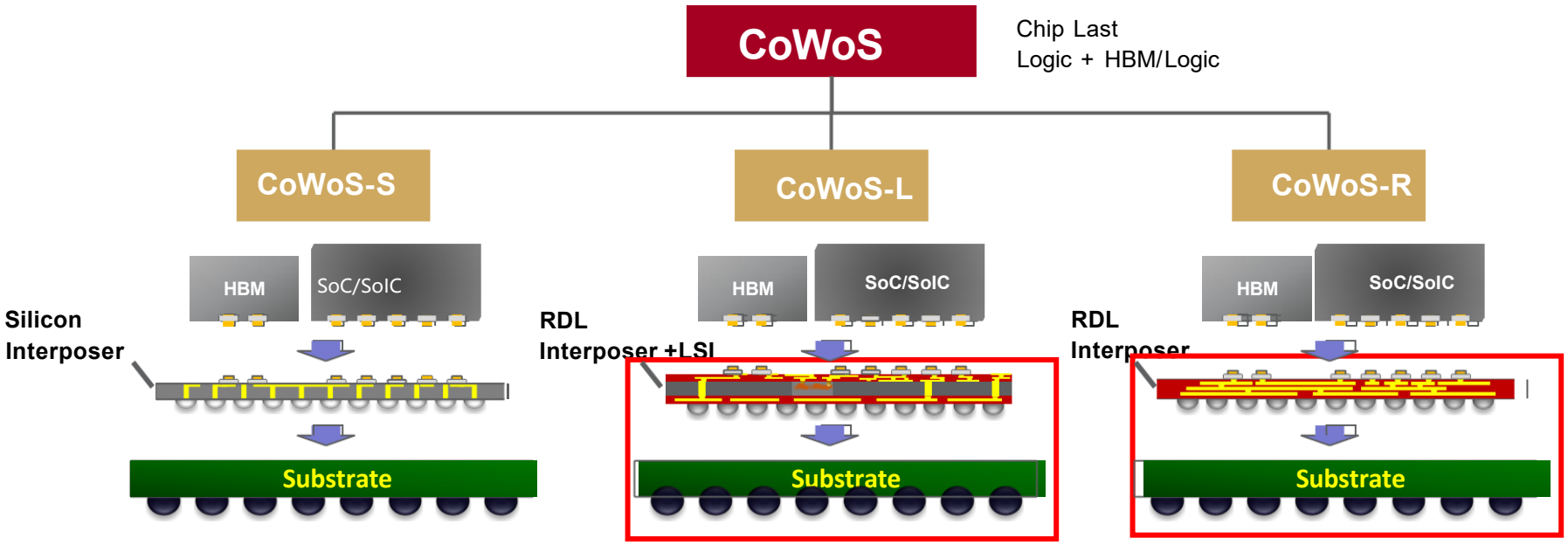
CoWoS® Enables AI Compute Scaling



Source: TSMC

CoWoS® Platform for HPC AI Applications

A Versatile 2.5D Packaging Technology for Heterogeneous Chiplet Integration



Source: TSMC

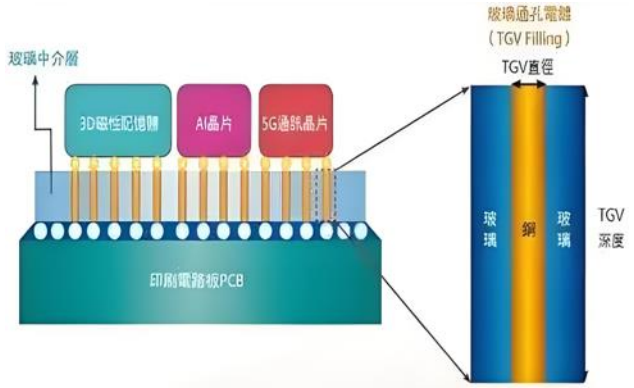
- **The red sections represent the TGV Substrate application; the overall package is a CoPoS application**

From TSV Silicon Substrates to TGV Glass Substrates

Driven by the demand for high-performance AI chips, glass substrate packaging is highly anticipated. The global IC packaging substrate industry is expected to reach $11.4 billion by 2025, and with the entry of manufacturers such as Intel, the replacement of silicon substrates by glass substrates will accelerate, with a penetration rate of over 20% within 5 years. Compared to silicon/organic substrates, glass substrate packaging technology is gradually becoming the future trend due to its superior material properties, such as high thermal stability, low dielectric constant, and high mechanical strength.

In advanced packaging, 2.5D and 3D IC integration solutions are a key component for achieving next-generation performance requirements and being suitable for commercial products. Ultra-high-density I/O connections can be achieved using interposers, with TSV being one of the most widely used interposer types.

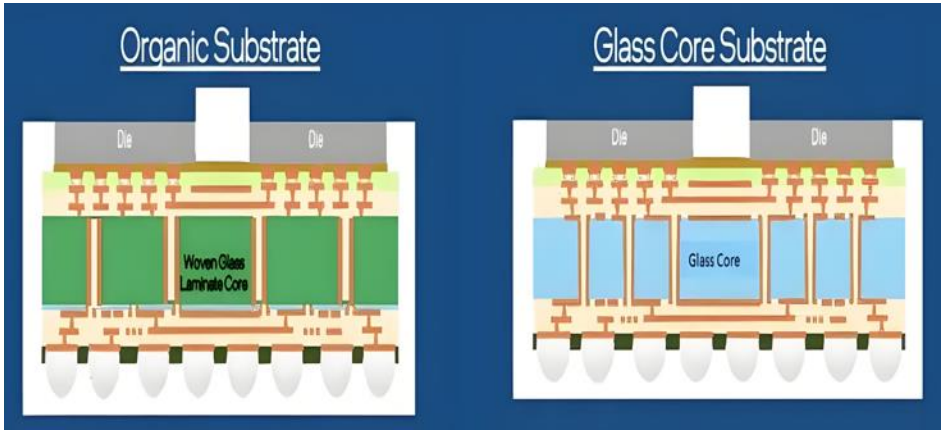
In glass substrates, vertical electrical connections are also provided through high-density vias, known as TGVs. Forming high-quality, high-density TGV is crucial for interposers. Recently, TGV technology has also been developed, replacing silicon interposers with glass interposers.

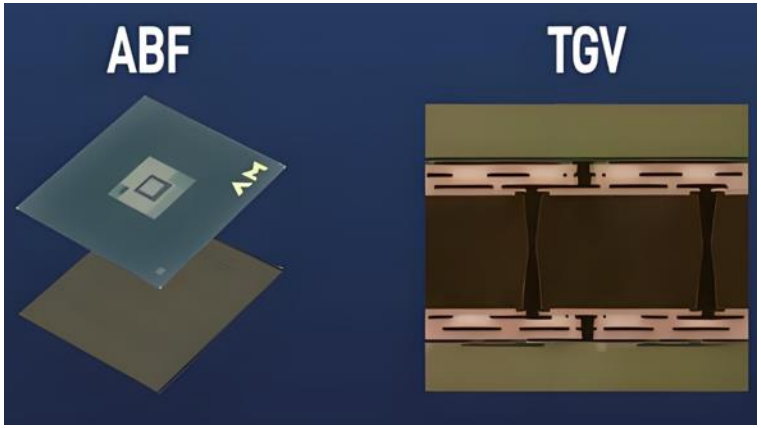


基板核心	硅	玻璃	有机材料	
			层压板	硅-金属化合物
表面粗糙度（nm）	＜10	＜10	400-600	＞1000
热膨胀系数（ppm/K）	2.9-4	3-9	3-17	16-30
杨氏模量（GPa）	165	50-90	10-40	22
吸湿性	0	0	0.04%	1-2.5%
热导率（W/m·K）	148	1.1	0.9	0.5-0.75
封装尺寸（mm）	35×35	100×100	70×70	50×50
面板/晶圆尺寸	300mm	710mm²	710mm²	300mm/510mm²

From Resin Substrates to Glass Core Substrates

The increasing complexity and performance requirements of integrated circuits are driving continuous innovation in packaging technology. Glass packaging, as an emerging packaging method, is rapidly gaining widespread attention. This includes technology and glass substrates.

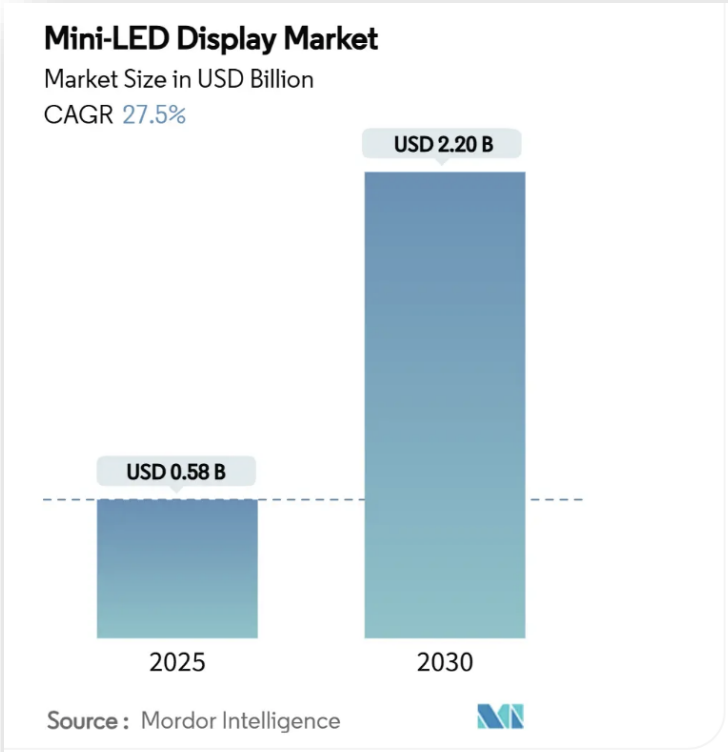




TGV technology has expanded into a wider range of applications. With the rise of emerging technologies such as 5G, artificial intelligence, and the Internet of Things, the requirements for packaging materials are becoming increasingly stringent. At this stage, TGV technology applications have covered multiple fields, including high-performance computing (HPC), millimeter-wave radar, optoelectronic sensors, and biosensors. Now, TGV technology not only focuses on achieving efficient vertical interconnects but also emphasizes improving process scalability and controlling manufacturing costs. For example, the industry is exploring ways to reduce TGV manufacturing costs through mass production, while also researching how to perform high-precision processing on larger glass substrates.

Global Mini LED Market Growth-Approximately 27.5% CAGR from 2025 to 2030

- The Mini-LED display market size is estimated at US$580 millions in 2025 and is expected to grow to US$2.2 billions by 2030, with a CAGR of 27.5% over the forecast period from 2025 to 2030



Market Overview

Study Period	2019 - 2030
Market Size (2025)	USD 0.58 Billion
Market Size (2030)	USD 2.20 Billion
Growth Rate (2025 - 2030)	27.50% CAGR
Fastest Growing Market	Asia Pacific
Largest Market	North America
Market Concentration	Medium

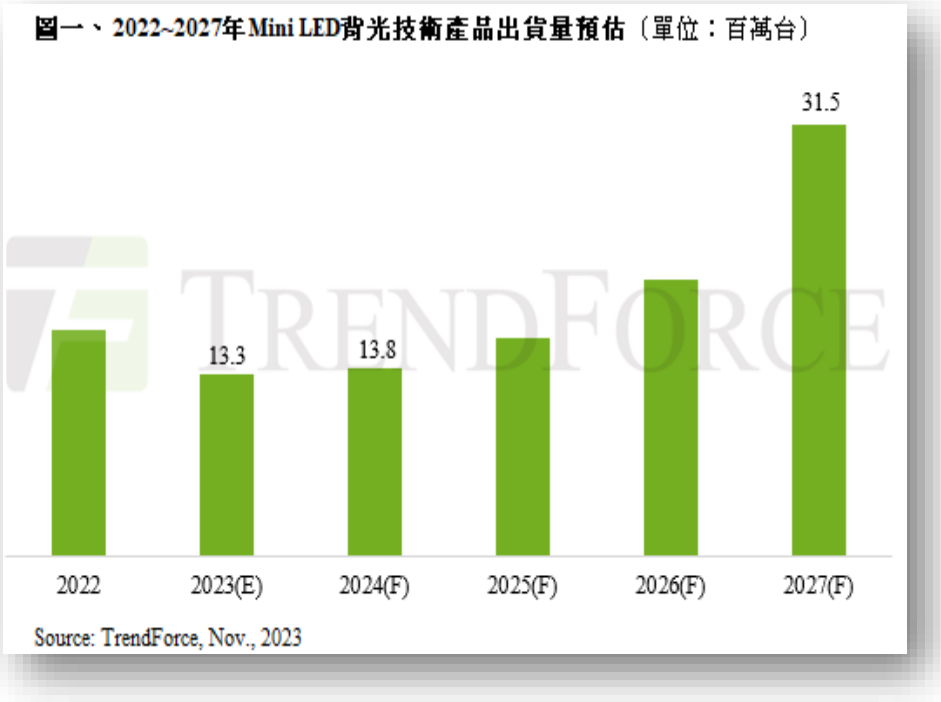
Major Players

LG Display SAMSUNG BOE AUO AUO MegaInsight

*Disclaimer: Major Players sorted in no particular order

Mini LED Backlight Module Shipments in 2022–2027 and 2030 Global Market Forecast

- According to the 2023 report of TrendForce, shipments of Mini LED backlight products will grow from approximately 13.3 million units in 2023 to approximately 31.5 million units in 2027, representing a CAGR of approximately 24%. Based on this, the Group anticipates that while the growth rate will slow slightly from 2028 to 2030, it will still maintain an annual growth rate of approximately 15%, with global backlight shipments reaching 48-54 million units in 2030, approximately three times that of 2025.



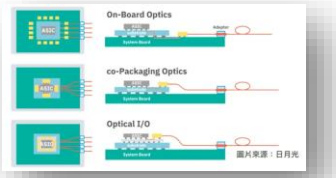
- **USD $200 is the average selling price.**
- **The global market for Mini LED backlight modules for displays is estimated at $6 billion by 2027, with TGV backlight modules projected to capture 5% of the market, representing a $300 million market.**

Business Model of TGV

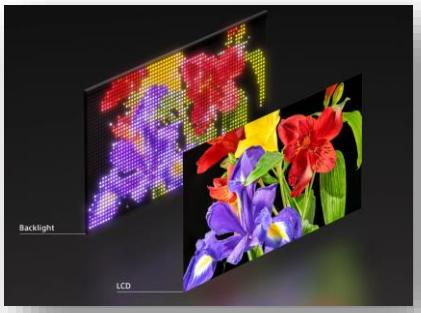
TGV Substrate

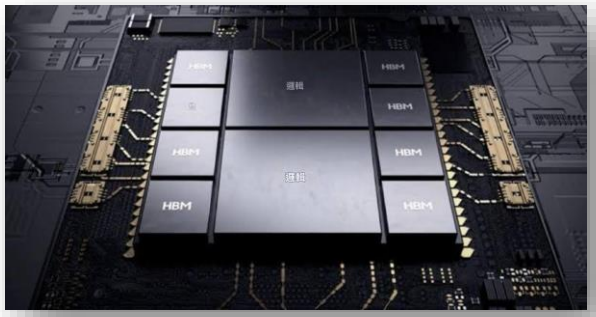
- Glass Core with Cu filling
  - Customer base: glass manufacturers, panel manufacturers, carrier board manufacturers, MLCC manufacturers
- Turn Key Solution (Process Flows + Equipment)
  - Military industrial enterprises
  - Special clients do not outsource products

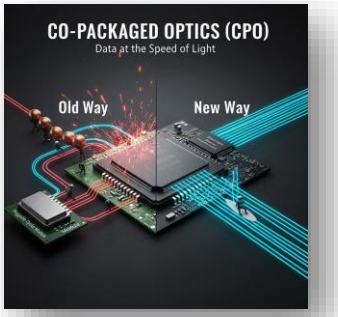
CoPoS



- CoB → CoG for Mini LED backlight module
- CoB → CoG for Mini LED direct display screen
- FOPLP for MLCC/ 2.5D/3D IC advanced packaging / HBM
- CPO for all professions and trades AI /Edge AI Server







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Key Technologies of Through-Glass Via (TGV) Processes

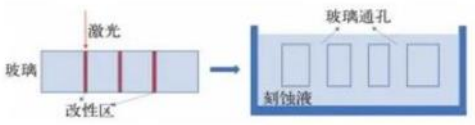
成孔技術

Phase II

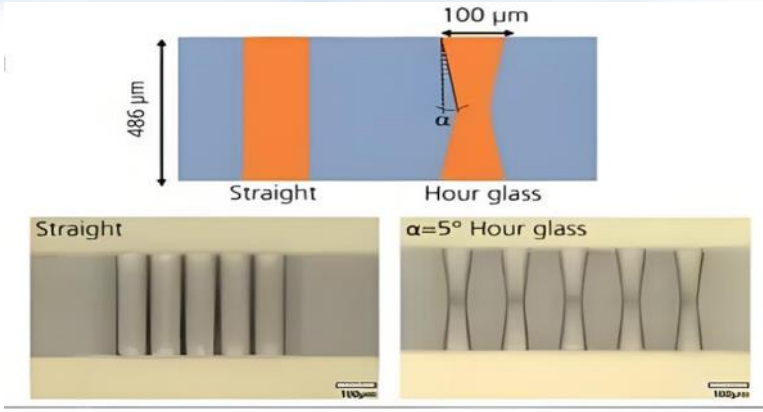
填孔技術

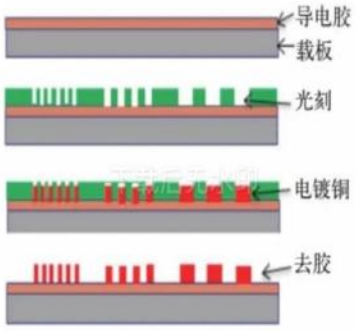
Phase I

高密度布綫



雷射改質蝕刻TGV





(a) RDL线路预制工艺

The red section represents the technology of CBTech TGV OEM line.

Concept of TGV Manufacturing Flow

Laser

- Method: Laser induced / Ultrashort-pulse laser
- Via diameter: 30–120 μm
- Blind Via > 20um
- Aspect ratio: ≤10:1
- Cleanliness: Debris-free after drilling

AOI

- Resolution: Sub> 1um
- Inspected parameters: Via location, diameter, and crack detection
- Inspection method: Optical/IR, optionally with AI detection

Cu Plating

- Type: Electroplating (DC or pulse)
- Thickness: depend on the customer's requirement
- Filling quality: Void-free via fill
- Additives: Leveler, accelerator, suppressor

Glass

- Material: Borosilicate / Fused Silica
- Thickness: >500um (typical)
- Size: Wafer 4"/ 6" / 8" / 12" & Panel 310x315, 510x515
- Surface: 20>=TTV>=1 um

Wet Etching

- Etchant: HF-based / Alkaline solution
- Purpose: Remove microcracks and debris
- Etch uniformity: Critical for Cu adhesion

Cu Seed

- Method: Sputtering / ALD / E-beam evaporation
- Adhesion: Good coverage in high-aspect-ratio vias
- Barrier layer: Optional (e.g., Ti or Ta)

TGV Manufacturing Line Specification

Panel Import AOI

- Surface Scanning (No Scratch/No Cracking/No Chipping)
- TTV<5um

Panel AOI

- Surface Scanning-
- (No Scratch/No Cracking/No Chipping)

01 02 03

Phase II

Panel THK Reduced (Out Source)

- HF / Alkali Etching
- Polish
- TTV<20um
- TTV<10 or 5um (option)

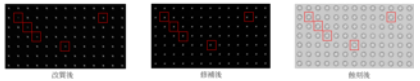
TGV Manufacturing Line Specification

Panel Cleaning

- Wet Bench
- Detergent + DIW
- IPA QDR (Dry-in/out)

Via Formation I

- AOI
- Leaser Induced Rework
- AOI



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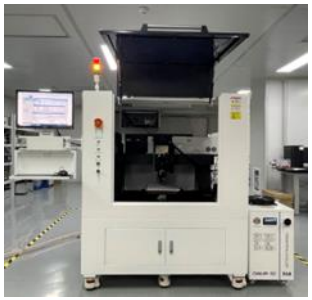
Via Formation I

- Laser Induced



Phase II

TGV Manufacturing Line Specification

Via Formation II

- Alkali Etching
- Wafer/Panel Comparable
- Waist: 35%~85%
- Highest AR: 100:950

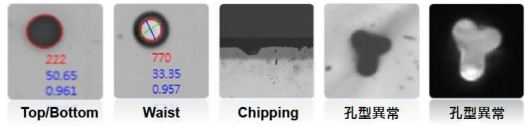
Via Cleaning

- Single/ Panel Vertical type
- Wafer/Panel Comparable
- IPA QDR (Dry in/out)

07 08 09

Via Formation AOI

- Wafer/Panel Comparable



Phase II

Phase I

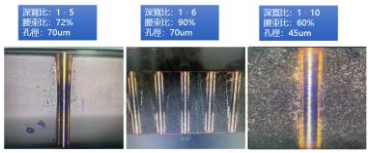
CBTech®

SUSTAINABLE DEVELOPMENT GOALS

TGV Manufacturing Line Specification

Via Metallization

- In-line Sputter
- Ti/Cu/TiW/Ni…..etc
- Wafer/Panel Comparable



Via Metallization Annealing

- Low Oxygen Heated (< 50ppm)
- < 400℃

10 **11** **12**

加工尺寸：最大510mm*515mm
加工玻璃厚度：0.1m-1mm
粗糙度Ra: 0.02-0.1um
孔径：30-100um
深宽比：10:1
镀膜均匀性：±5%
镀膜附着力：5B

Phase I

Via PTH Cu

- Wafer/Panel Comparable
- Bench Type
- E-Less
- Single Type (AR> 1:10)

TGV Manufacturing Line Specification

Via Metallization AOI (CIP)

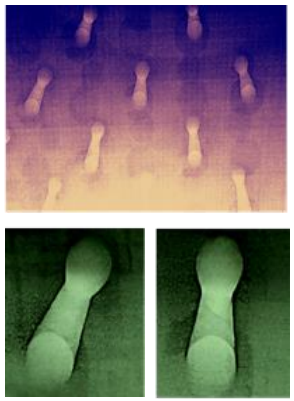
- X-Ray / CT / New Method
- Resolution > 2um

Via Cu Annealing

- Low Oxygen Heated (< 50ppm)
- < 400℃

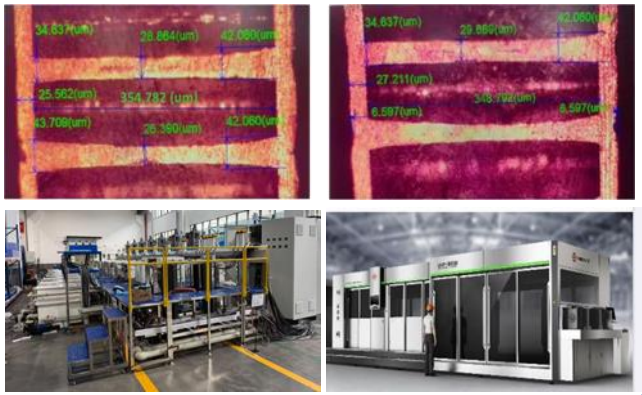
13 → 14 → 15

Phase I



Via Cu Filling

- Single Vertical Plater
- Wafer/Panel Comparable
- PR+DC w/ CuO & insoluble anode
- IPA QDR (Dry in/out)
- Dimple< 5um
- Chemicals in-house
- Plater can for Single/Double side



TGV Manufacturing Line Specification

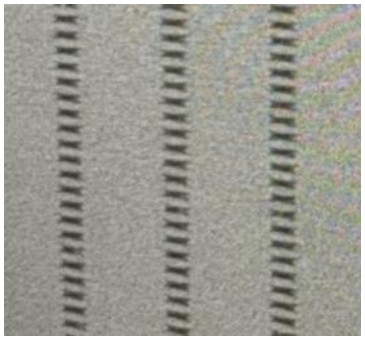
Via Filling AOI

- 2D X-ray
- 3D X-ray Resolution>10um
- Resolution <10um (Option)

Cu THK / Surface Modification

- Grinding / De-plating

16 17 18



Cu THK AOI

- Electrical Method

TGV Manufacturing Line Specification

PR Coater

- Spin/Slit Tyes
- Wafer/Panel Comparable
- Matched w/ LDI or Stepper
- CLN/Coater/Pre-Q/Expo/Post-Q/Dep./AOI

RDL Formation

- DES: Developer/Etcher/Stripper
- Developer: Na2CO3/TMAH
- Etcher: Non-H2O2 base
- Stripper: NaOH or Organic base
- Single vertical type
- Match for Single/Double side
- Max Panel: 800*800
- L/S: 10/10um (5/5um Y2025/E

19 → 20 → 21

Patent Expo.

- AOI
- Leaser Direct Image
- L/S >= 10/10um
- Y2026/E L/S>=5um

TGV Manufacturing Line Specification

RDL Formation AOI

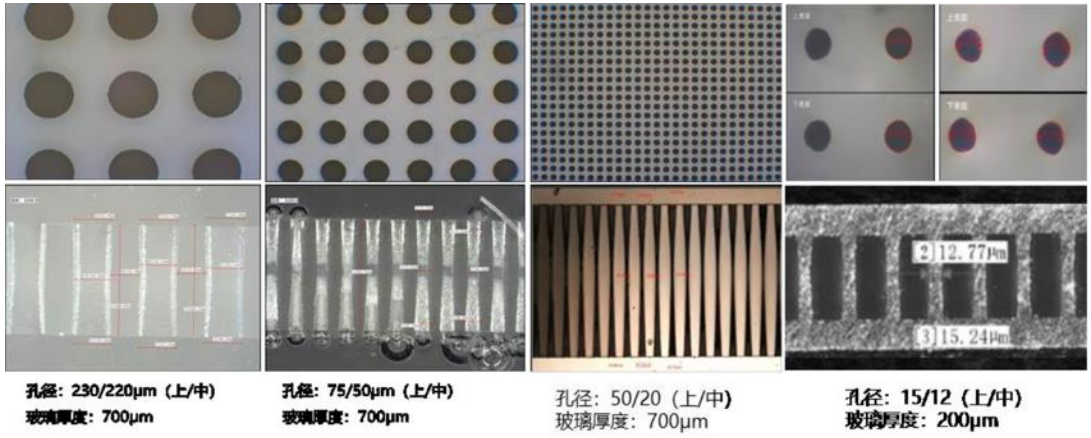
- AOI + Electrical Test

22 → 23 → End

Panel Export CLN

- Wet Bench
- Detergent + DIW
- IPA QDR (Dry-in/out)

TGV Process Capability & Performance Index



TGV SVM OEM production line capacity: 500 pieces/month

Glass size: Maximum 510mm x 515mm

Glass thickness: 100μm - 1000μm

Hole aspect ratio: 850μm 1:10 capability is achieved; 1000μm 1:10 breakthrough is underway

Hole diameter: ≥3μm

Through-hole spacing: ≥10μm

Taper: 0°-15° (controllable)

Non-matrix dense hole one-time forming

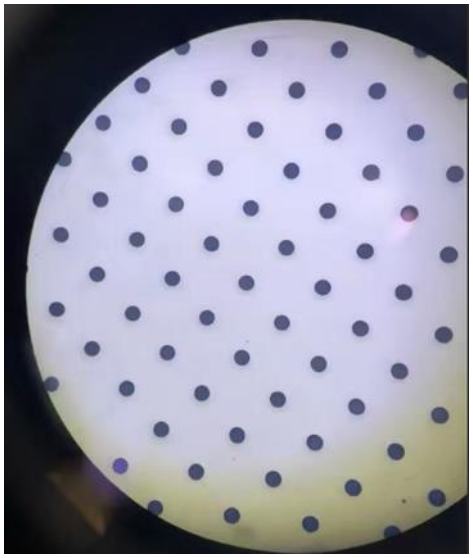
Dimensional accuracy ±5μm

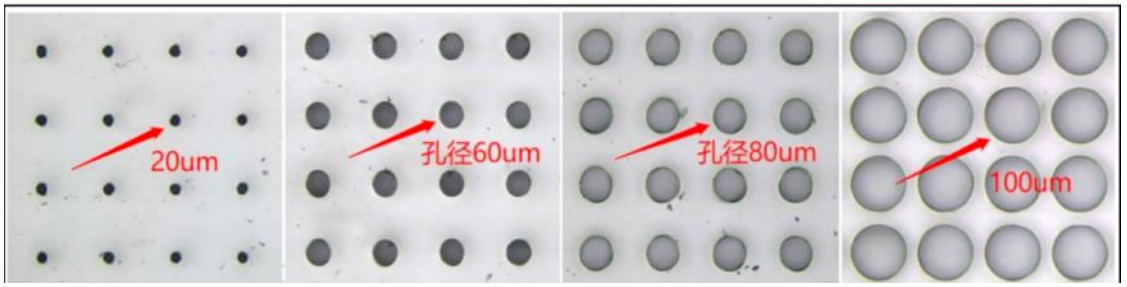
Universal compatibility with different glass types

Capability for both through-hole and buried hole processing

TGV Process Capability & Performance Index

Laser-modified etched samples





Technical Capabilities:

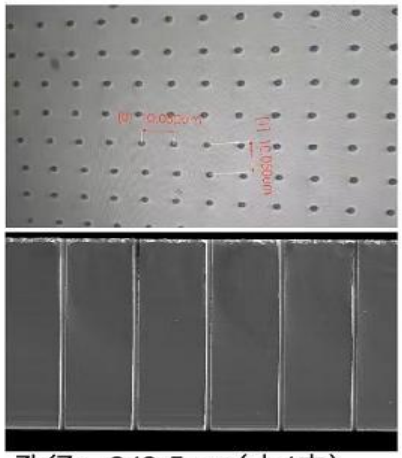
Minimum Aperture: 10μm corresponding to standard 200μm

Glass Thickness: 100μm - 1000μm (maximum)

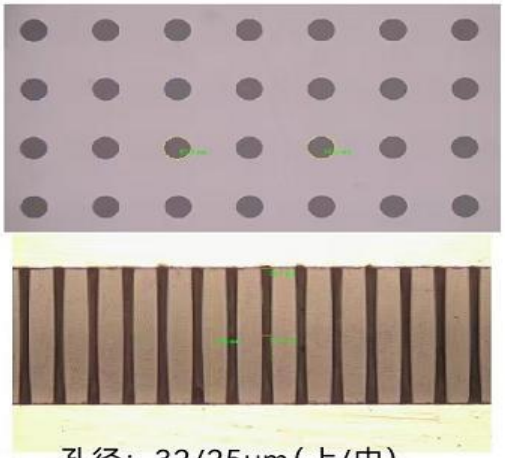
Through-hole Spacing: >10μm

Taper: 0°-15° (controllable)

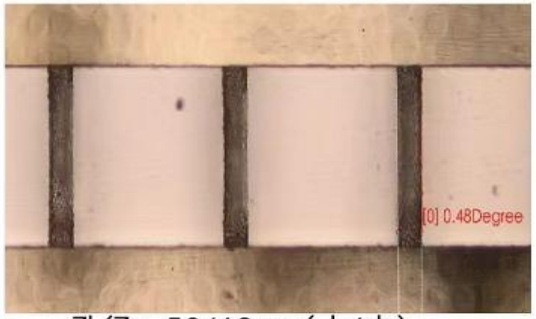
TGV Process Capability & Performance Index



孔径：3/2.5μm（上/中）
厚度：300μm



孔径：32/25μm（上/中）
厚度：450μm



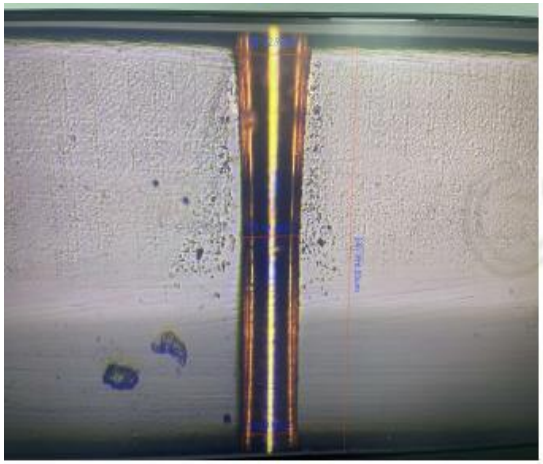
孔径：50/48μm（上/中）
厚度：460μm
垂直孔

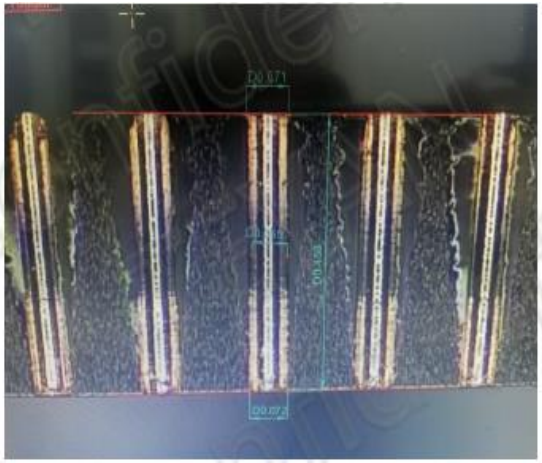
孔径：92/53μm（上/中）
厚度：500μm
锥度可控

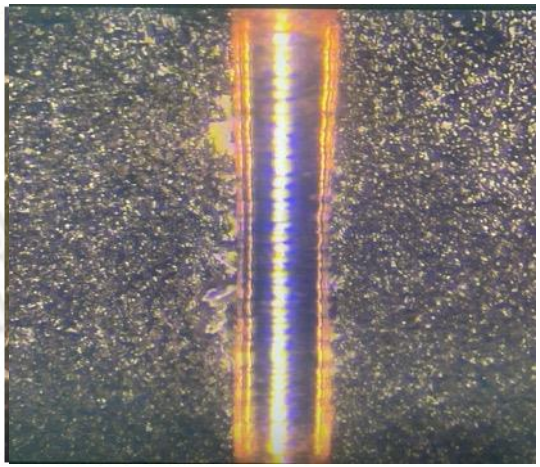
TGV Process Capability & Performance Index

TGV seed layer Sputter AR

Aspect ratio: 1 : 5 Waist-to-hip ratio: 72% Aperture: 70μm	Aspect ratio： 1 : 6 Waist-to-hip ratio： 90% Aperture： 70um	Aspect ratio： 1 : 10 Waist-to-hip ratio： 60% Aperture： 45um

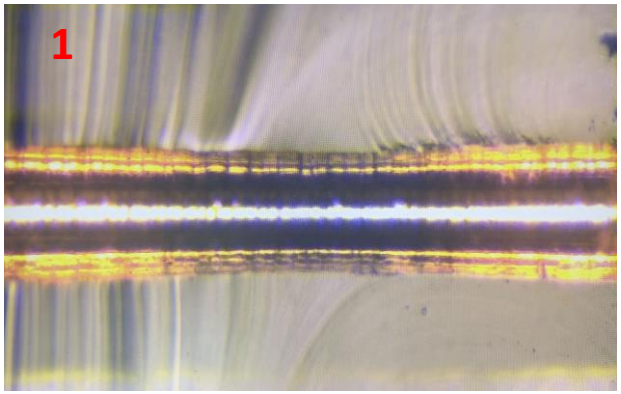


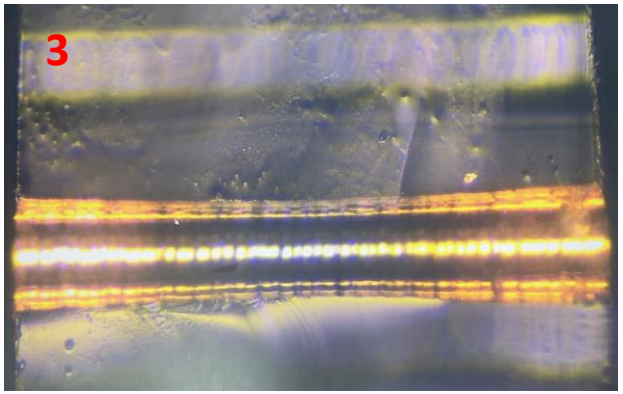


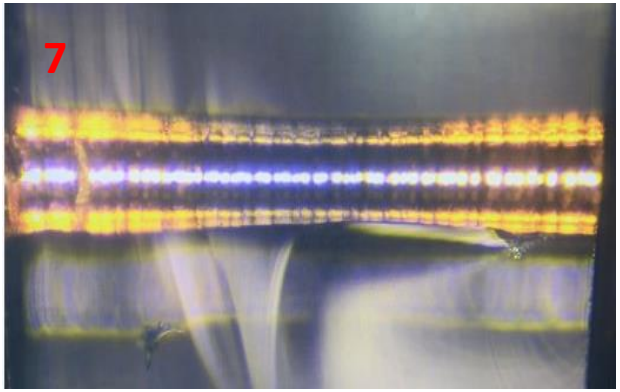


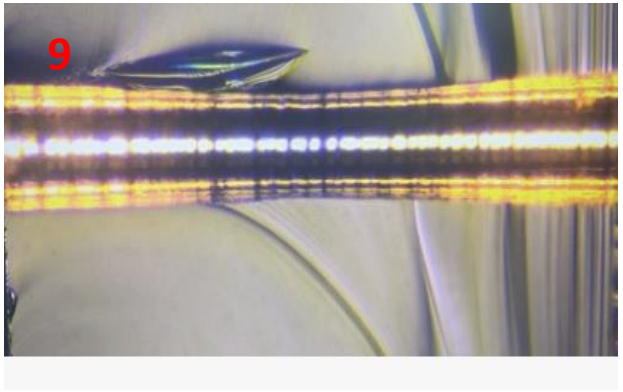
TGV Process Capability & Performance Index

Sputter 850µm 1:10 Slices



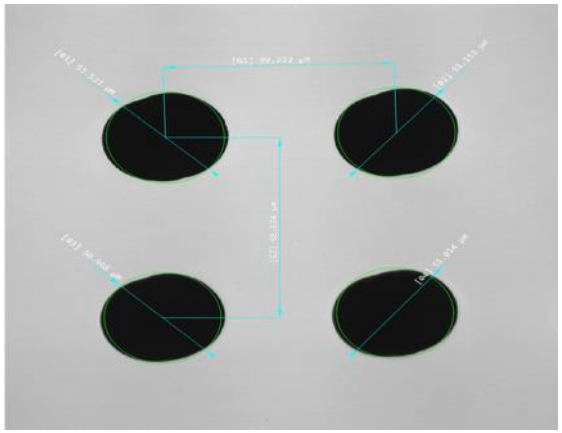




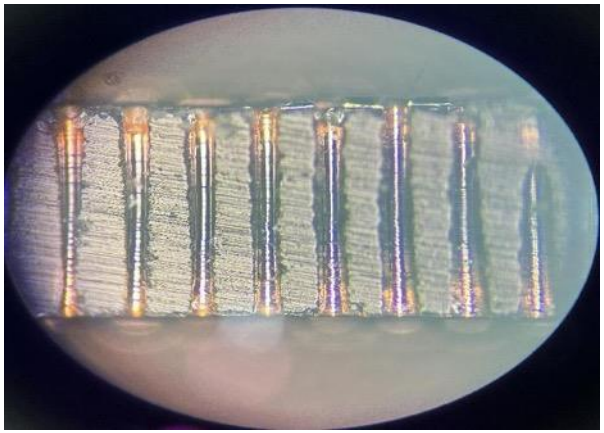


TGV Process Capability & Performance Index

Sample parameters:
Aperture 50μm, Spacing 100μm



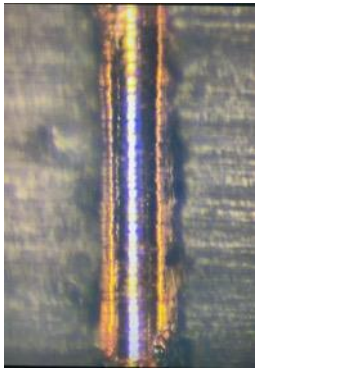
Before Sputter

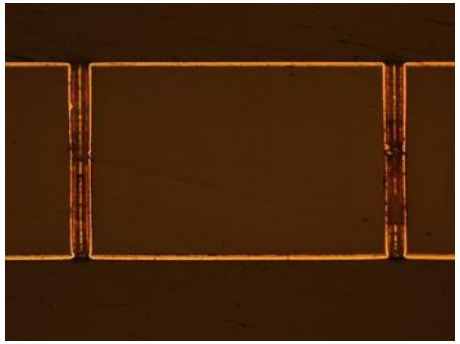


Slices after Sputter

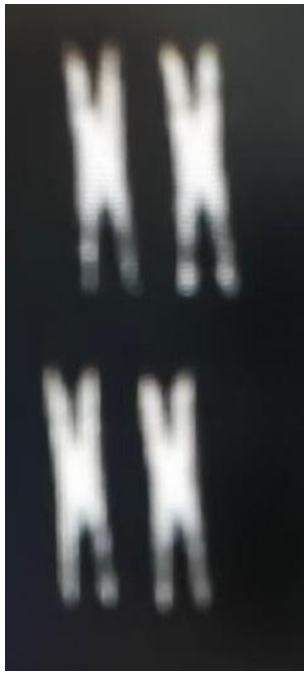
The resistance was 0.6 MΩ measuring by multimeter after Sputter

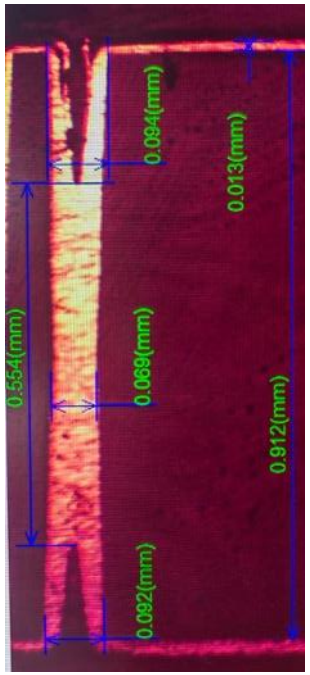
TGV Process Capability & Performance Index



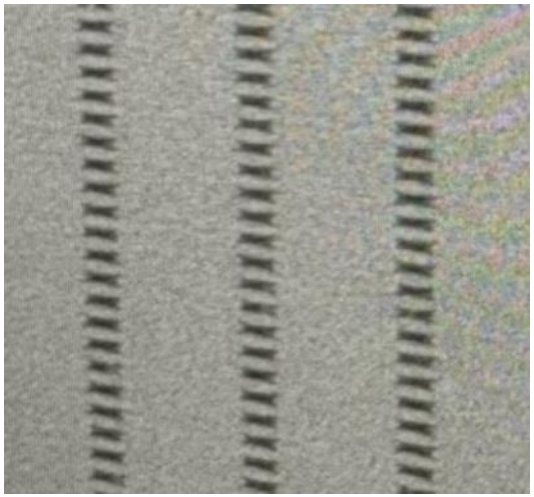


70/630um Sputter





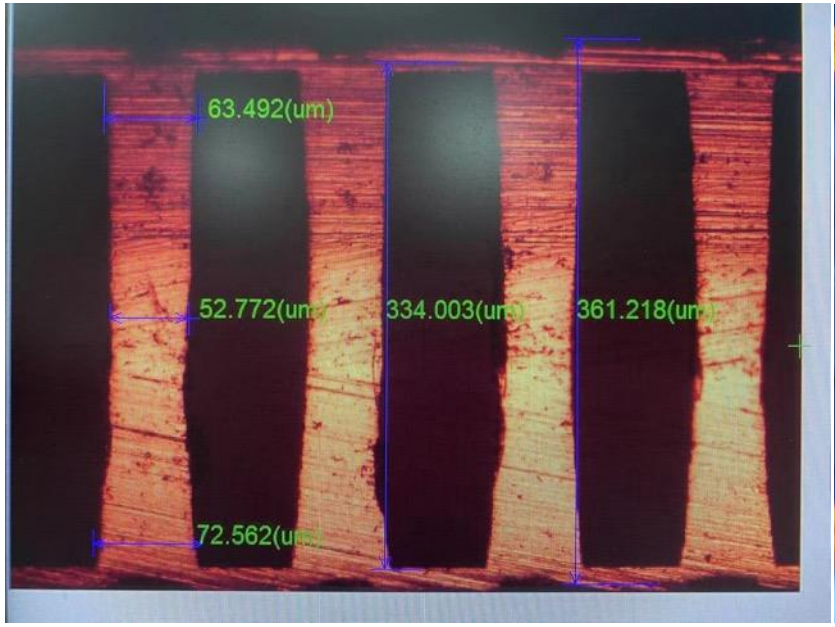
100/900um Sputter/PTH/Cu Plating



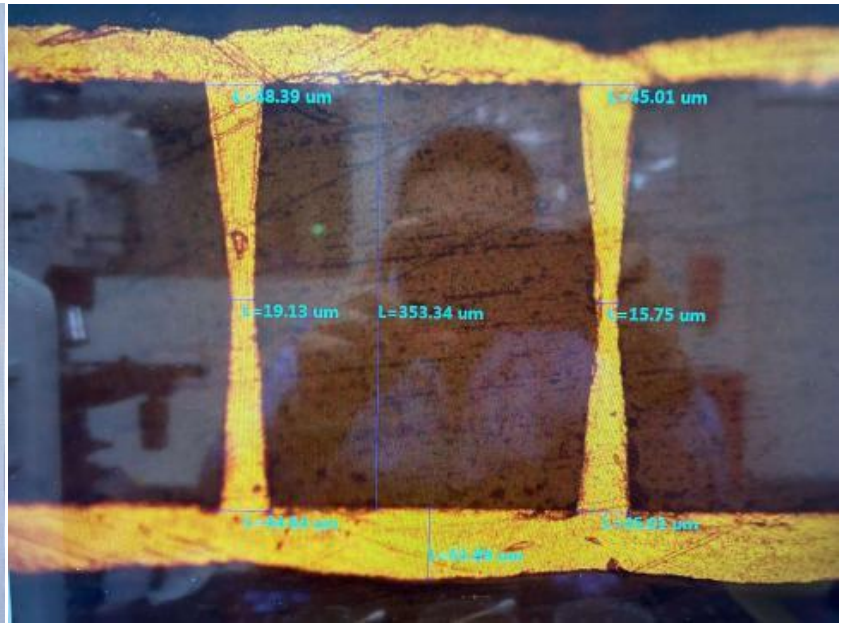
100/600/10um Cu Plating

TGV Process Capability & Performance Index

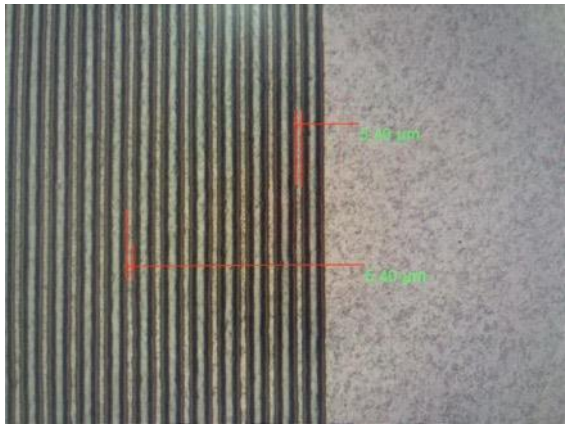
Waist-to-hip ratio：72%

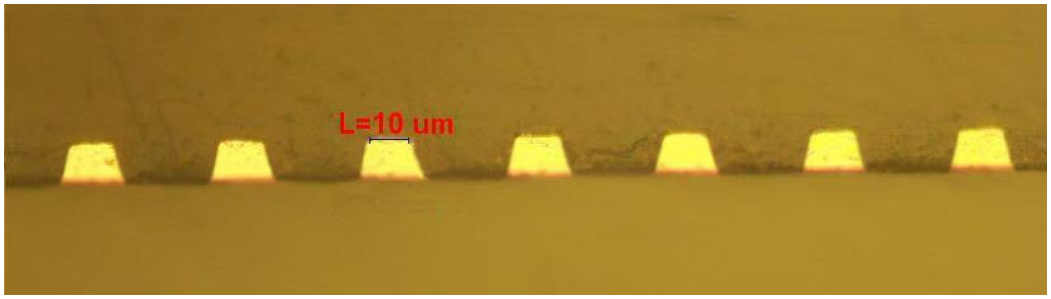


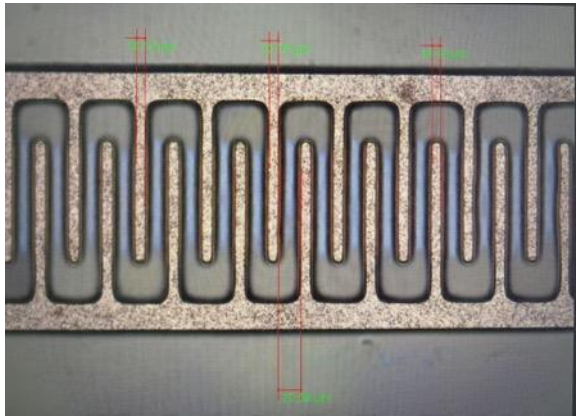
Waist-to-hip ratio： 35%

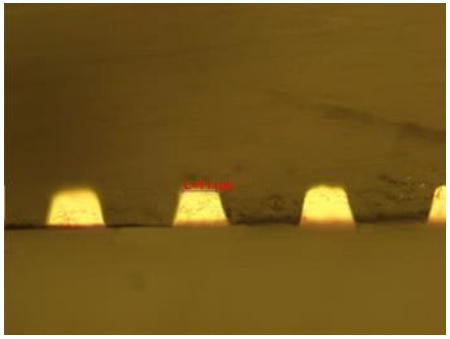


TGV Process Capability & Performance Index







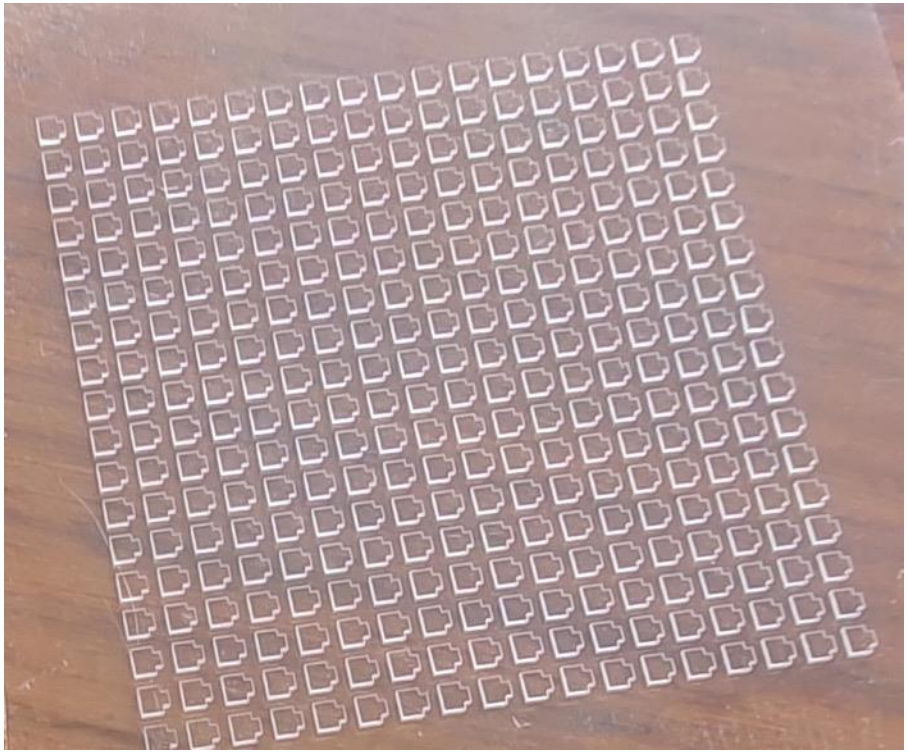


Copper thickness: 15μm
Photoresist: 15μm
Line spacing: 20μm

5 um RDL W / Etching Back

TGV Process Capability & Performance Index

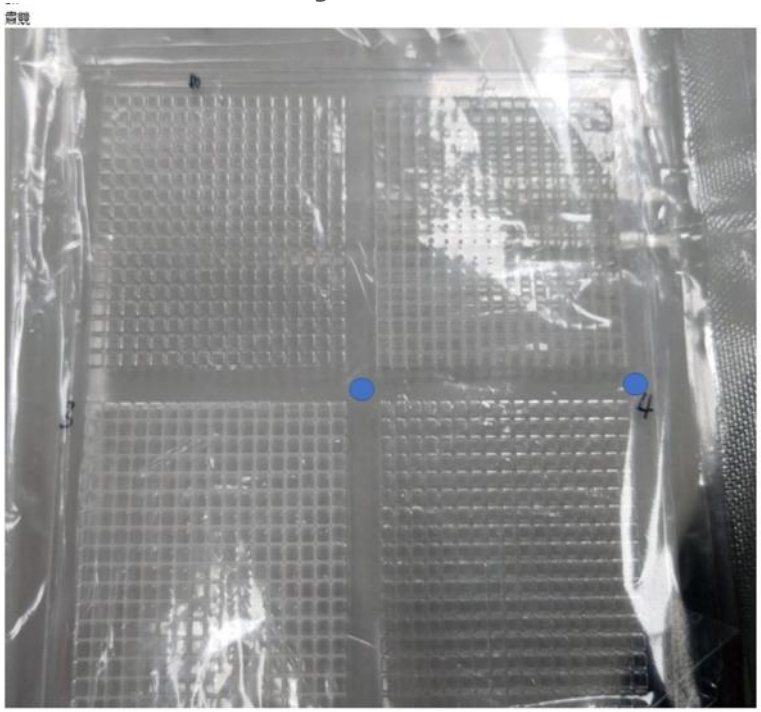
- 1600μm w/ BVH & TH
- Capable for Face up & Face down Chip attcahed



- Sophie Laser Induced is on going

TGV Process Capability & Performance Index

- **Visual representation of CPO/TGV glass panel surface roughness uniformity test**



- **Thickness Measurement Layouts – CPO/TGV Glass Substrates**

K-EDGE	2.17	3.28	34.60
T-CENTER	1.77	2.85	37.50

- The surface roughness at four crosshair measurement points (center/edge) on the substrate are tested. The measurement result error is ±10 µm / 10 µm.
- Measurement (center/edge) is required on both the front and back sides of the substrate – the same locations are symmetrically tested on the front and back sides, for a total of 4 locations.

TGV Production Line Scene



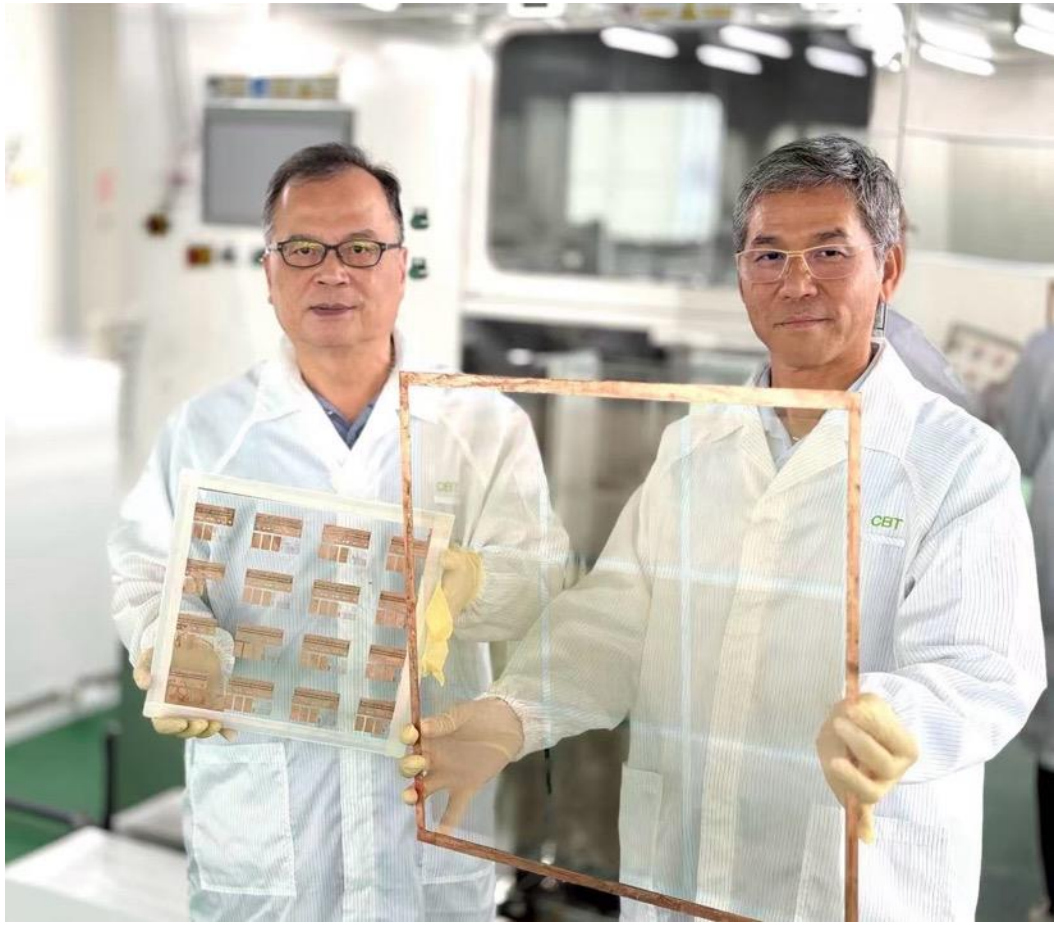




CBTech®

SUSTAINABLE DEVELOPMENT GOALS

TGV Production Line Scene



Outline

- Introduction to the Company and its Existing Products
- Overview and Business Model of TGV Glass Substrate Market
- **CBTech**
  1. TGV Glass Substrate Metallization Manufacturing Line
  2. **Photomask AOI**
- Subsidiary- BHT
  1. Semi Equipment PEALD/PEALE
  2. Front, Back-End IC Test & Packaging
- Q & A

Mask AOI Product Agent

- **Major clients (Asia/Global)**
  - Taiwan Mask Corporation (TMC) – Taiwan
  - Photronics – Asia fabrication service / Global facilities
  - Dai Nippon Printing (DNP) – Japan
  - HOYA Corporation – Japan （Includes Reticle/Mask Detection and Solutions）

- **Foundry / IDMs**
  - TSMC （Taiwan）
  - UMC （Taiwan）
  - SMIC （China）
  - Samsung / SK Hynix （South Korea）

- **Packaging / Testing / Substrate / Advanced Packaging**
  - **OSAT :** ASE,SPIL & JCET
  - **Substrate/PCB manufacturing :** Ibiden （Japan）, Unimicron, Kinsus, ZhenDing
  - **Advanced Packaging / Interposer**

Company	Country	-
Dai Nippon Printing (DNP)	Japan	
Toppan Photomasks (Teks Cend)	Japan	
Photronics, Inc.	USA	
Hoya Corporation	Japan	
Taiwan Mask Corporation (TMC)	Taiwan	
Compugraphics	UK/Euro	
SK-Electronics	South Korea	
LG Innotek	South Korea	
Nippon Filcon	Japan	
Advance Reproductions Corporation	USA	
Infinite Graphics Incorporated	USA	
HTA Photomask	—	

Stratus Vision Mask AOI

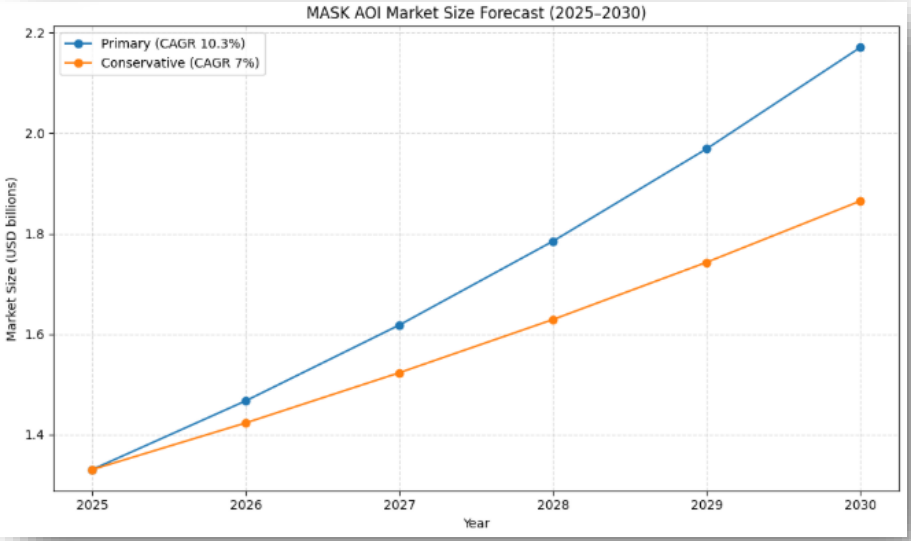
Stratus Vision specializes in AOI and precision inspection equipment, suitable for a variety of advanced materials and packaging processes, including:

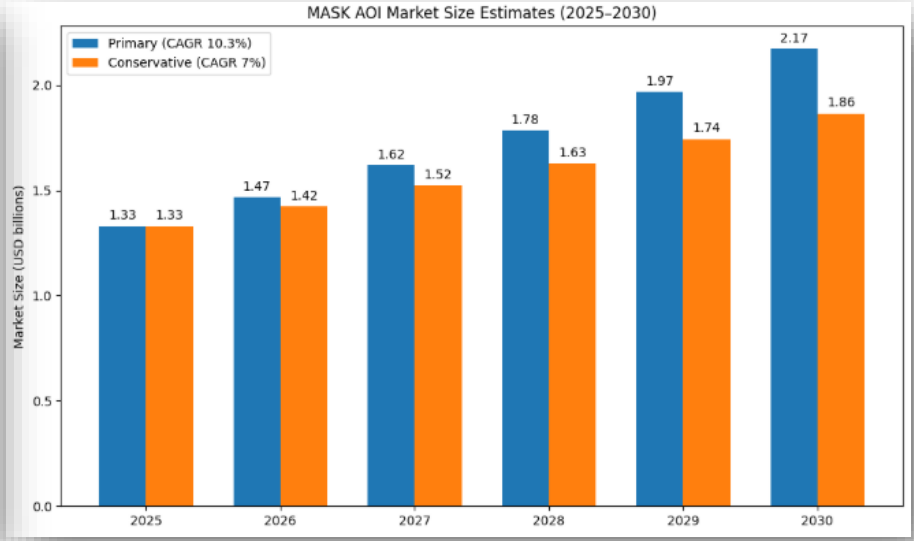
- Electronic component inspection
- Ceramic packaging LTCC/HTCC
- Substrate inspection
- Wafer surface and structure inspection
- Reticle defect inspection

Supports both in-line and offline multimodal detection requirements

Mask AOI Market Size: CAGR of over 10% from 2025 to 2030

- MASK AOI（Automated Optical Inspection）Global Market Size: The global MSAK is estimated at US$1.33 billion in 2025 and is expected to grow to US$1.86 billion by 2030, with a CAGR of over 10% during the forecast period.





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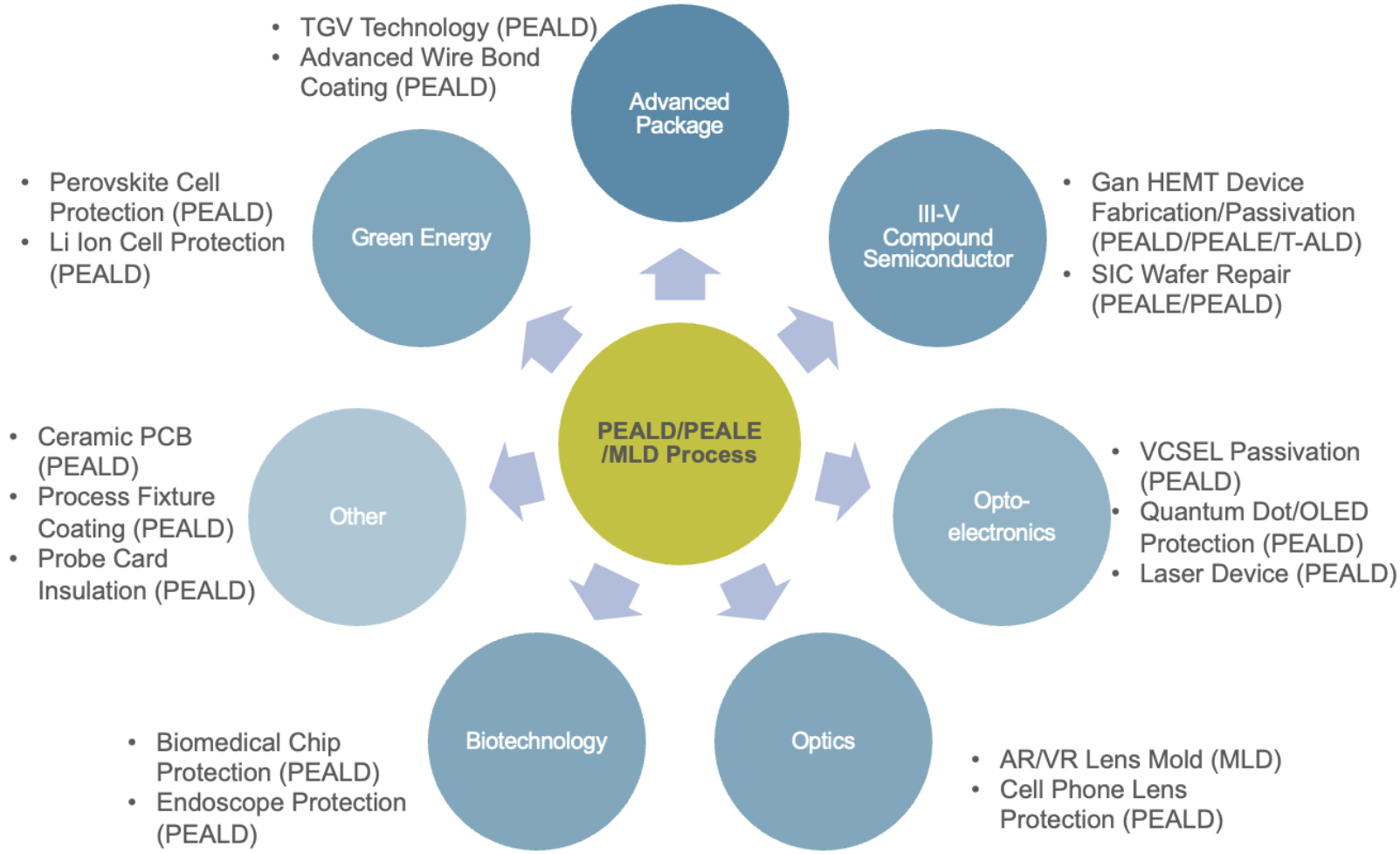
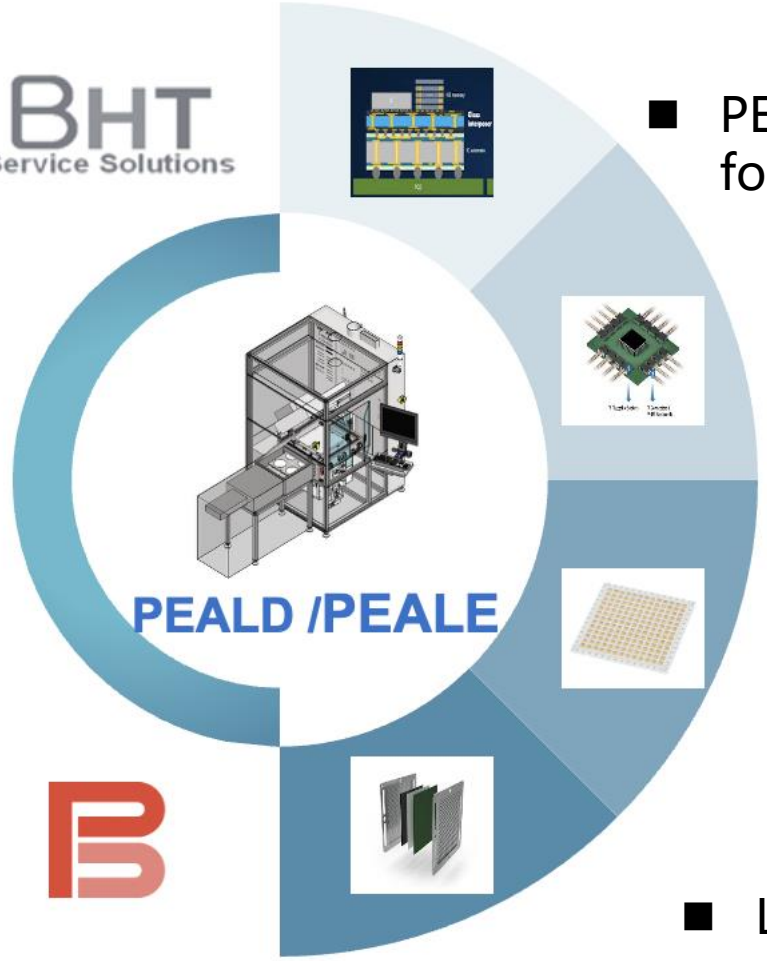
BHT / BP PEALD / ALE Application Areas

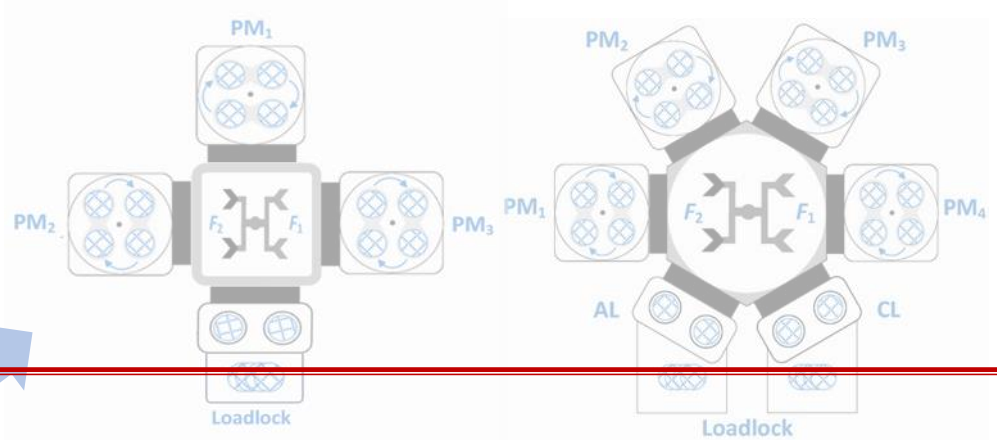


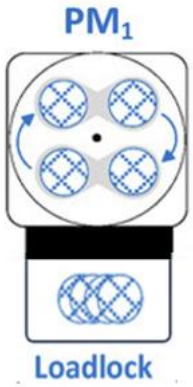
BHT / BP PEALD / PEALE Focused Application Areas



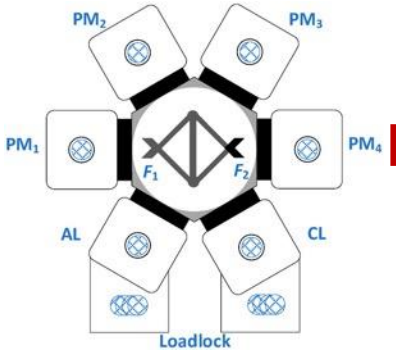
- PEALD Cu Seed Layer in Glass Interposer for Advanced Packaging
- High-Efficiency Silicon Photonics with Low-Loss PEALD Coatings & PEALE Smoothing
- High-Performance Ceramic Heat Conductive Substrate
- Low-Carbon Solid Oxide Fuel Cell

Concept Of BHT / BP PEALD / ALE Multi-space Process Modules

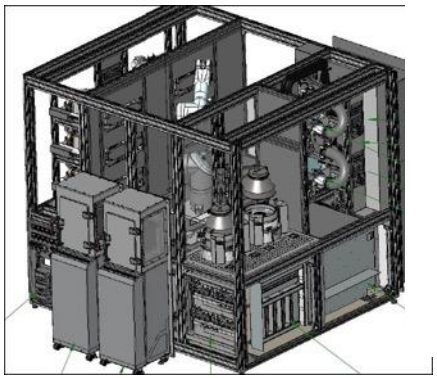


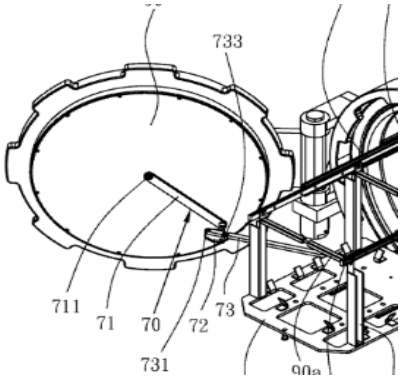


SINGLE



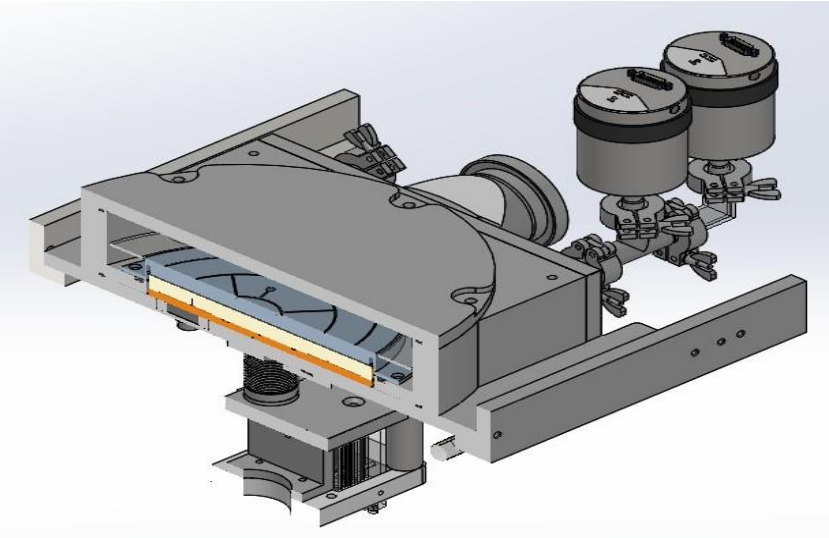
CLUSTER

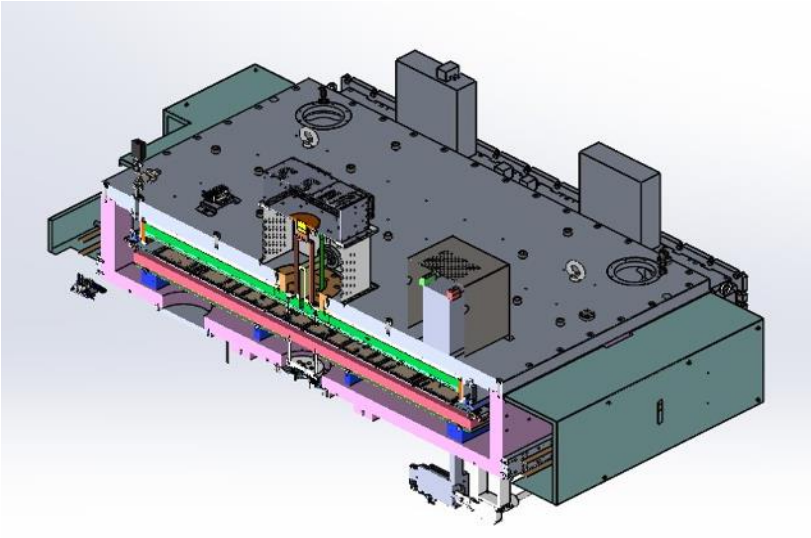




CONCEPT OF MULTI-CHAMBER AND BATCH TYPE

BHT PEALD / ALE System With Flexible Modular Design

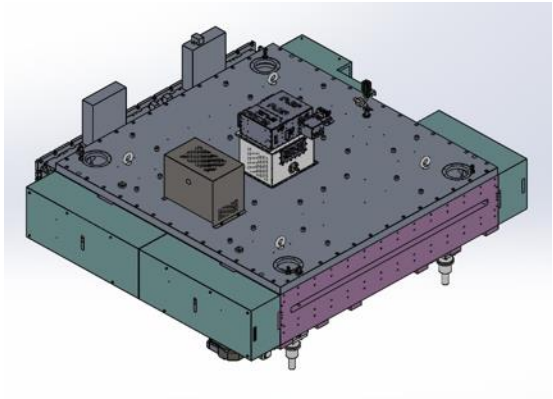




- BHT PEALD / ALE system adopts a flexible modular design, which can fully support a variety of substrate sizes:
  - Wafer：150 mm、200 mm、300 mm
  - FOPLP / TGV：310 × 315、510 × 515mm
  - Panel Glass：310 × 315、510 × 515、600 × 600mm

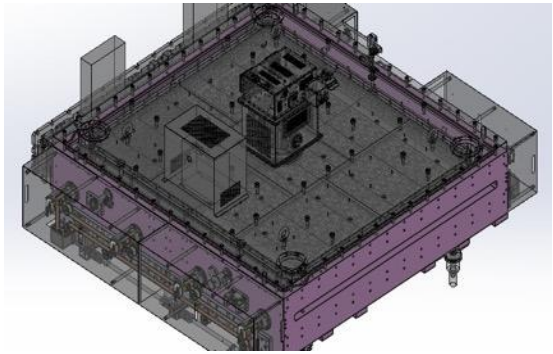
Specifically Designed for Cu Seed Layer Applications in TGV Glass Through-Hole Applications

- **Chamber, Vacuum & Gas Delivery System**
  - Applicable glass substrates: 310×310 / 510×515 / customized sized
  - Base Pressure：1×10^{-6} Torr rating
  - Cavity Temperature range：50–350°C（Ramp rate 2–5°C/sec)



- **Precursor Delivery**
  - Cu ALD Precursor（for example: Cu amidinate / Cu guanidinate)
  - Co or TiN can be selected as the barrier layer

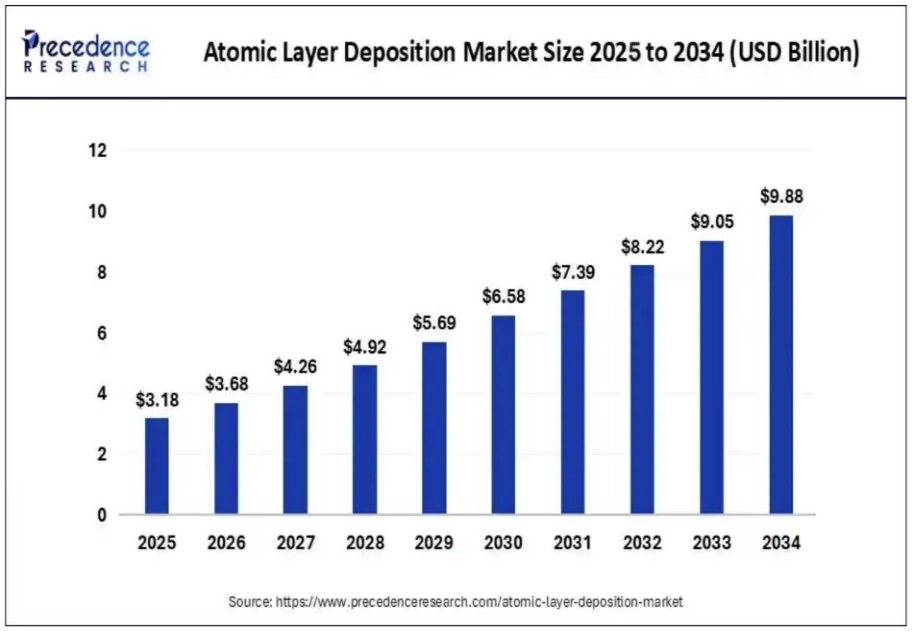
- **Plasma System — Optional for PEALD**
  - ICP/CCP Plasma Source（13.56 MHz / 2–3 kW)
  - Plasma uniformity：within ±3%



- **Cu ALD Seed Layer Performance**
  - Film thickness uniformity：< ±2%
  - Conformality：> 95% in TGV
  - Aspect ratio; 1:10 ~1:20
  - Resistivity < 5–10 μΩ•cm

Atomic Layer Deposition Equipment Market Trends: PEALD/ALE Future Market Demand and Growth (2025-2034): Approximately 13.42% CAGR

- **The Global Atomic Layer Deposition Market Size** Is Calculated At **USD 3.18 Billion In 2025** And Is Predicted To Increase From **USD 3.68 Billion In 2026 To Approximately USD 9.88 Billion By 2034, Expanding At A CAGR Of 13.42% From 2025 To 2034.**



Report Coverage	Details
Market Size in 2025	USD 3.18 Billion
Market Size in 2026	USD 3.68 Billion
Market Size by 2034	USD 9.88 Billion
Growth Rate from 2025 to 2034	CAGR of 13.42%
Base Year	2025
Forecast Period	2025 to 2034
Segments Covered	Product, Application, Region
Regions Covered	North America, Europe, Asia-Pacific, Latin America, and Middle East & Africa

- **BHT is dedicated to the development of advanced packaging (TSV/TGV, RDL), ceramic heat dissipation substrates, and other material modification processes and application equipment.**

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BHT Back-end Packaging and Testing Equipment Solutions

- Q&R and Burn-In Systems and Applications
- IOL (Intermittent Operating Life) System
- SCAD Smartbox (A Flexible Remote Solution For HTOL / THB / HTRB Tester Monitoring)

SYNERGIES CAD BURN IN TESTER BUSINESS APPROACHES

Regional Service Agent Phase I

Strategic Partnership Asia

Phase II.

Phase III

Regional Sales Representative Include Service

Marketing Strategy :

- ODM / OEM Design service
- Training courses – Provide Technical support Before/After

Customer Base :

- IC Designer, IC Wafer Maker, IC Packing & Test

Small RA Lab

OEM/ODM IC Testing Service

Marketing Strategy

- "One-Stop solution" – Quick, Correct, Optimized
- Quick Delivery Logistic Service (QDL)

Customer Base :

- IC Designer, IC Wafer Maker, IC Packing & Test
- Government and Academic R&D Project Department

Regional Contract Equipment Manufacturing

Contract Scope :

- Manufacturing on a contract basis, Excluded Software & Driver Board basically,
- BHT specialize in simply manufacturing physical products, but some are also able to handle a significant part of the design and customization process if needed.
- Synergies companies focus on product innovation, design and Sales.

Q&R and Burn-In Systems and Applications

High performances over a wide range of solutions

- High precision Very Low Voltage (less than 0.5V)
- Medium-High Power (2kW/slot)
- Very High Voltage (3kV)
- Width Temperature Rage LTOL at -55˚C, HTOL (up to 220˚C)
- PTC (Power Temperature Cycle)
- Modular Thermal Chambers with multiple independent zones

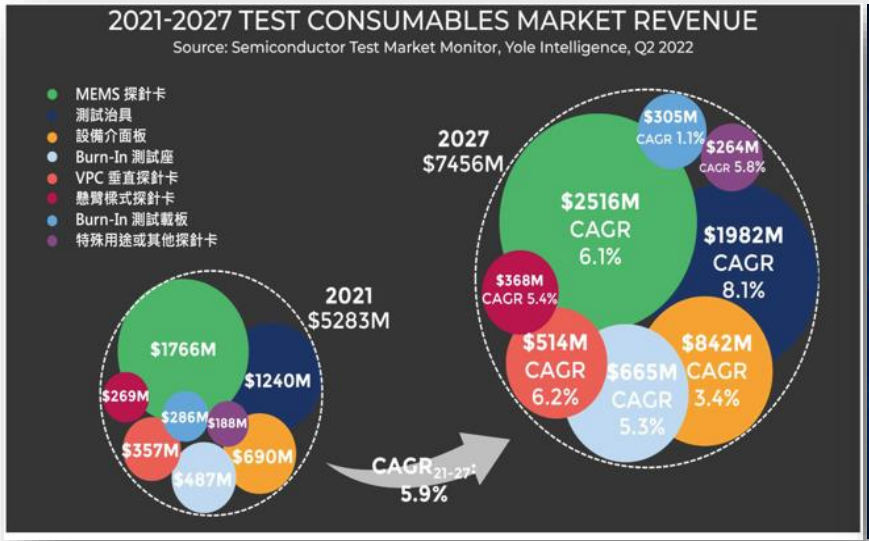
Q&R Applications coverage

Model	HTOL	LTOL	HTRB	THB	PTC	BURN-IN
CUBE 480	√	√	√		√	√
CUBE 700	√	√	√		√	√
Tower 75K	√		√	√		
Tower 75K SS	√		√	√		
CUBE NeXt	√	√	√		√	√

Q&R and Burn-In Systems and Applications

Specification Category	Description	Key points for CoWOS/AI chip testing
Voltage	High precision Very Low Voltage (less than 0.5V)	Key trends in AI chips: The core voltage of high-performance AI chips continues to decrease (Vcc < 0.5V), which places extremely high demands on the voltage accuracy of testing equipment. This is a key capability to ensure accurate testing.
Power	Medium-High Power (2kW/slot)	High power density trend: CoWoS's integrated AI/HPC chip consumes extremely high power (hundreds to thousands of watts). 2kW/slot demonstrates its ability to handle high-power testing, which is crucial for testing advanced AI chips.
Temperature	Very High Temperature HTOL (up to 220◦C)	Accelerated Reliability: Increasing the test temperature (HTOL) is a standard method for accelerating the long-term reliability verification of wafers. A capability of 220°C demonstrates its ability to test the most demanding high-temperature application scenarios
Thermal	Modular Thermal Chambers with multiple independent zones	CoWoS Heterogeneous Integration Challenges: The CoWoS package contains multiple dies (logic, HBM, etc.). Independent temperature control zones enable differentiated temperature control testing for different areas, simulating a more realistic operating environment.
Models	**Key Specifications and Applications**	**Key points for CoWOS/AI chip testing**
CUBE 480 / 700 / NeXt	Features with high pin-count and high parallelism, with NeXt possessing very high pin-count and analog features.	Pin count and parallelism: CoWoS integration of AI/HPC chips and HBM memory requires extremely high I/O pin count. High parallelism means the ability to test a large number of chips simultaneously, which is key to meeting the needs of mass shipments of AI chips and shortening mass production timelines.
Tower 75K (HTRH/HTRB)	Integrates with existing climate chambers to conduct temperature, humidity, and stress tests (THB/HAST).	Environmental reliability: CoWoS packaging materials are complex and sensitive to changes in humidity and temperature. THB/HAST is an important test to ensure that the package can still operate reliably in extreme environments (such as the humid and hot environment of a data center), and is a long-term stability indicator that investors are concerned about.

Burn-in Test System Demand and Growth: Approximately 8.9% CAGR from 2023 to 2031



Market Trends	Specific Requirements	SCAD Related System Specifications	Remark
Extremely high chip power consumption	High power handling and heat dissipation capabilities	Medium-High Power (2kW/slot), HTOL up to 220◦C, Modular Thermal Chambers	Ensuring the ability to test high-heat/high-power AI/HPC chips
Energy saving and performance requirements	Ultra-low core voltage supply with extremely high precision	High precision Very Low Voltage (less than 0.5V)	Meeting advanced process and low-voltage testing requirements, with high technical barriers
CoWoS heterogeneous integration	Extensive I/O pin testing and analog function verification	Very high pin-count, Analog features (CUBE NeXt)	Determining whether the equipment can test advanced AI packages integrating HBM and logic
Massive shipment demands	High-efficiency, high-throughput aging screening	High parallelism (CUBE 480/700/NeXt), BURN-IN coverage	Shortening time-to-market (TTM) and improving production efficiency
Increasingly complex packaging structures	Rigorous environmental and thermomechanical stress reliability testing	PTC, THB/HTRB (Tower 75K/SS)	Verifying the long-term stability of CoWoS/SiP packages in extreme environments

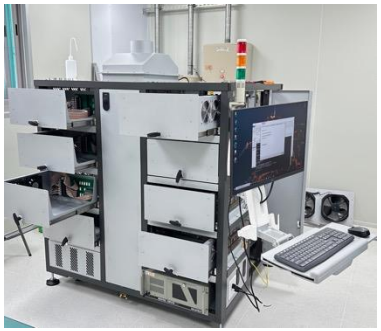
Category III WBG Semiconductor Reliability Testing Equipment
IOL (Intermittent Operating Life) System

Key Features

- **High Voltage Withstand Voltage Testing Capability and Comprehensive Reliability Verification Mechanism**

  As server power architectures have increased from 54V to 800V, traditional silicon-silicon (Si) components are gradually being replaced by GaN/SiC.
  This system can perform accelerated life testing, including endurance tests such as IOL (Ingress-Order) testing, to verify the reliability of devices under high-voltage environments. It rigorously tests the behavior of GaN/SiC power devices under high voltage, high frequency, and high temperature conditions. The system ensures the stability and reproducibility of reliability verification results and evaluates device degradation behavior and lifespan performance.

- **Application Value: The system can provide reliability and lifetime data for GaN/SiC power devices, and is suitable for**
  - AI server power modules
  - Datacenter power architecture
  - Electric vehicle (EV) power systems
  - Industrial control and power supply equipment, etc



- **Standard-oriented system design**

  Supports operating environments up to 800V, and can perform
  - Pressure resistance verification
  - Heat tolerance test
  - High-speed switching characteristic life verification

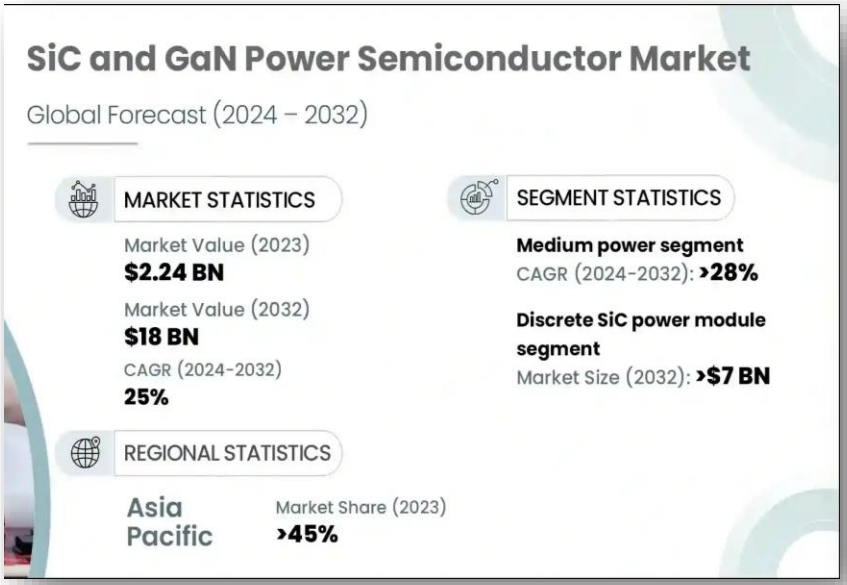
  Meets the needs of next-generation power semiconductor applications.

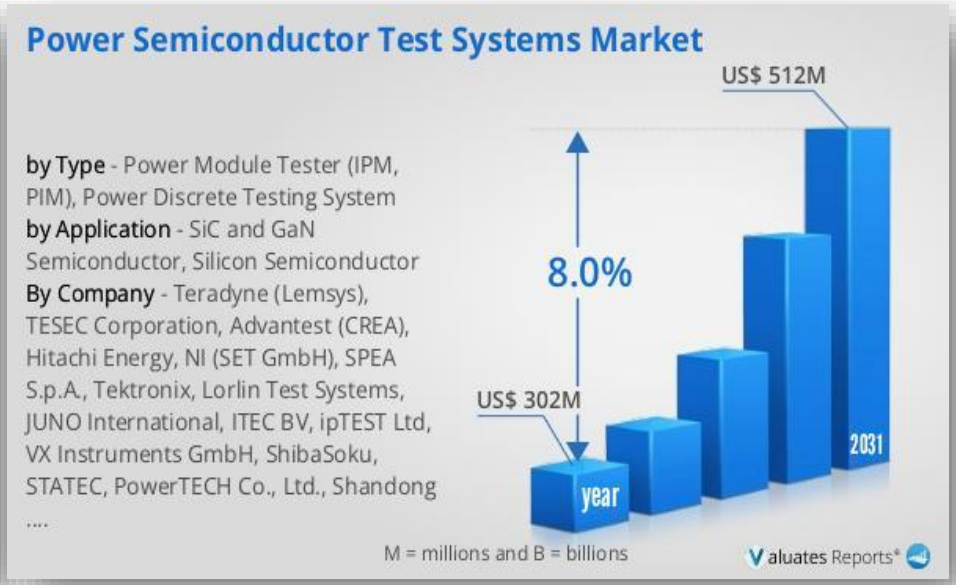
Category III WBG Semiconductor Reliability Testing Equipment
IOL (Intermittent Operating Life) System

Items	Specifications
Test Capacity (Number of Channels)	80 CH, multiple drawers compatible with standard housing sizes, customizable for different substrates
Maximum Current Capacity	20A heating current per CH for discrete component testing
Test Form Factor	No burn-in required, custom substrates (suitable for multiple packages)
Cooling System	Intelligent fan temperature control: 6000 rpm × 4, dynamic on/off temperature control + dual temperature confirmation by IR thermal imager and RTD monitoring
Material Support	Open test platform suitable for testing Si/SiC/GaN
Test Standards	Testing according to AQG 324 and AECQ-101 test guidelines for the same application scope
Tj Measurement	Currently using NI high-speed acquisition card for measurement (1 μs sampling)
Flexibility Applicable	High (customized small boards)
Applications	Laboratory reliability verification

The Total Market for Semiconductor Reliability Testing Systems is Projected to Grow at Approximately 8.0% CAGR from 2023 to 2031

- **Power Semiconductor Test Systems Market Size :**
  The global market for Power Semiconductor Test Systems was valued at US$ 302 million in the year 2024 and is projected to reach a revised size of US$ 512 million by 2031, **growing at a CAGR of 8.0%** during the forecast period.

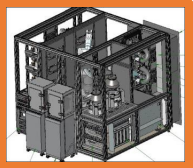




CBT Group 4 Core BUs

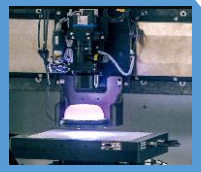
PCB Equipment BU

Semi Equipment BU



TGV BU

Semi Mask BU



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Enabling Smart Manufacturing
Through IT Ecosystem Innovation

Thank You for Your Attention !

Q & A